Low-Voltage, Low r_{ON}, Dual DPDT Analog Switch

FEATURES

- Low Voltage Operation (2.0 V to 5.5 V)
- Low On-Resistance @ 2.7 V - r_{ON}:
  SW_1, SW_2 - 3.2 Ω
  SW_3, SW_4 - 0.64 Ω
- Fast Switching: t_{ON} = 46 ns
  t_{OFF} = 21 ns
- QFN-16 (4x4 mm) Package

BENEFITS

- Space Saving Solution
- Low Power Consumption
- Guaranteed Low Voltage Operation
- Low Voltage Logic Compatible

APPLICATIONS

- Cellular Phones
- Integrated Speaker Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

DESCRIPTION

The DG2017 is a dual DPDT (double-pole/double-throw), optimized for high performance analog switching, and specifically designed to benefit portable audio applications.

One pair of double-throw switches is sub 1 Ω for low impedance speaker performance while the second pair of double-throw switches is suitable for microphone applications.

With the DPDT configuration, the DG2017 provides the flexibility for stereo-single-end or differential BTL output structures with a fully integrated differential microphone switching solution.

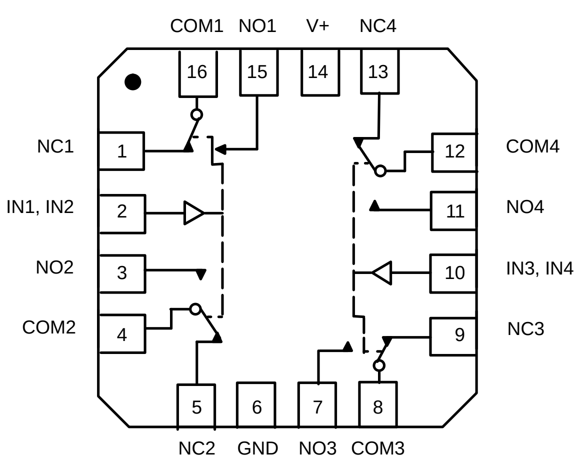
The DG2017 is an integrated monolithic device in a QFN-16 (4 x 4 mm) package that provides a space saving solution over the use of multiple single SPDT devices as well as providing the advantage of on-resistance flatness and matching that single SPDT devices cannot offer.

The DG2017 provides low charge injection (2 pC), fast switching time (t_{ON} and t_{OFF} less than 100 ns), excellent Off-Isolation and Crosstalk (–70 dB @ 100 kHz). During operation, continuous current through any or all switches is rated at ±200 mA, ideal for portable audio applications.

Built on Vishay Siliconix's low voltage CMOS process, the DG2017 contains an epitaxial layer that prevents latchup. Break-before-make is guaranteed. When on, each switch conducts equally well in both directions, and block up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

QFN-16 (4 X 4)



Top View

TRUTH TABLE		
Logic	**NC1, 2, 3 and 4**	**NO1, 2, 3 and 4**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	16-Pin QFN (4 x 4 mm)	DG2017DN

ABSOLUTE MAXIMUM RATINGS

Reference to GND
V+ . . . . -0.3 to +6 V
IN, COM, NC, NO[a] . . . . -0.3 to (V+ + 0.3 V)
Current (Any terminal except NO, NC or COM) . . . . 30 mA
Continuous Current (NO, NC, or COM) . . . . ± 200 mA
Peak Current . . . . ± 300 mA
(Pulsed at 1 ms, 10% duty cycle)
Storage Temperature (D Suffix) . . . . -65 to 150°C
Package Solder Reflow Conditions[d]
16-Pin QFN (4 x 4 mm) . . . . 240°C

Power Dissipation (Packages)[b]
QFN-16 (4x4 mm) . . . . 1880 mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 23.5 mW/°C above 70°C
d. Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10%, V_{IN} = 0.4 or 1.6 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
DC Characteristics							
On-Resistance	r_{ON} (SW_1, SW_2)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		3.2	3.7 4.3	Ω
	r_{ON} (SW_3, SW4)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.67	1.1 1.2	
r_{ON} Flatness[d]	r_{ON} (SW_1, SW_2)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		1.4	2.0	
	r_{ON} (SW3, SW_4)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.12	0.3	
r_{ON} Match[d]	Δr_{ON} (SW_1, SW_2)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full			0.3	
	Δr_{ON} (SW_3, SW_4)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full			0.3	
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 0.3 V/3.0 V V_{COM} = 0.3 V/3.0 V	Room Full	-0.5 5.0		0.5 5.0	nA
	$I_{COM(off)}$		Room Full	-0.5 5.0		0.5 5.0	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}=V_{NC} V_{COM} =0.3 V/3.0 V	Room Full	-0.5 5.0		0.5 5.0	
Digital Control							
Input High Voltage	V_{INH}		Full	1.6			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance	C_{in}		Full		6		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	-1		1	µA

SPECIFICATIONS (V+ = 3 V)

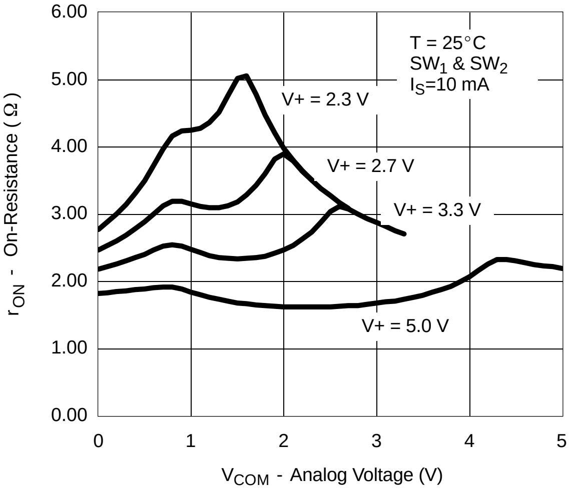
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10%, V_{IN} = 0.4 or 1.6 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Dynamic Characteristics							
Turn-On Time	t_{ON}, (SW_1, SW_2)	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF (Figure 1,2)	Room Full		62	85 91	ns
	t_{ON}, (SW_3, SW_4)		Room Full		46	74 79	
Turn-Off Time	t_{ON}, (SW_1, SW_2)		Room Full		12	35 36	
	t_{ON}, (SW_3, SW_4)		Room Full		21	46 48	
Break-Before-Make Time	t_d, (SW_1, SW_2)		Full	5	45		
	t_d, (SW_3, SW_4)		Full	5	26		
Charge Injection[d]	Q_{INJ}, (SW_1, SW_2)	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω (Figure 3)	Room		2		pC
	Q_{INJ}, (SW_3, SW_4)				1		
Off-Isolation[d]	OIRR, (SW_1, SW_2)	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz (Figure 4)	Room		-68		dB
	OIRR, (SW_3, SW_4)				-51		
Crosstalk[d]	X_{TALK}, (SW_1, SW_2)				-69		
	X_{TALK}, (SW_3, SW_4)				-51		
N_O, N_C Off Capacitance[d]	C_{OFF}, (SW_1, SW_2)	V_{IN} = 0 or V+, f = 1 MHz	Room		12		pF
	C_{OFF}, (SW_3, SW_4)				43		
Channel-On Capacitance[d]	C_{ON}, (SW_1, SW_2)				86		
	C_{ON}, (SW_3, SW_4)				283		
Power Supply							
Power Supply Range	V+		2.0			5.5	V
Power Supply Current	I+	V_{OE} = 0 or V+				1.0	μA

Notes:

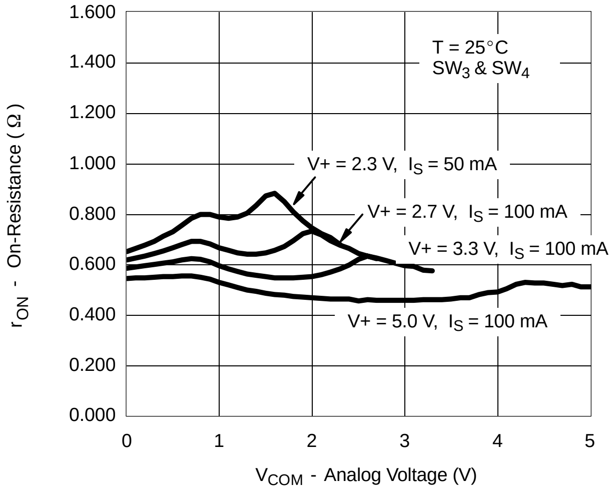
a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

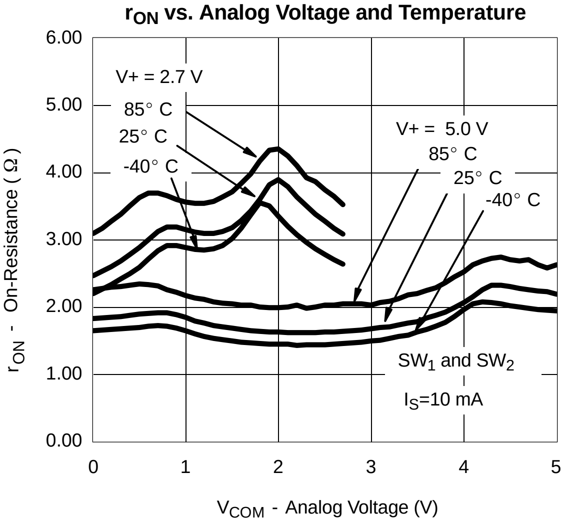
r_{ON} vs. V_{COM} and Single Supply Voltage



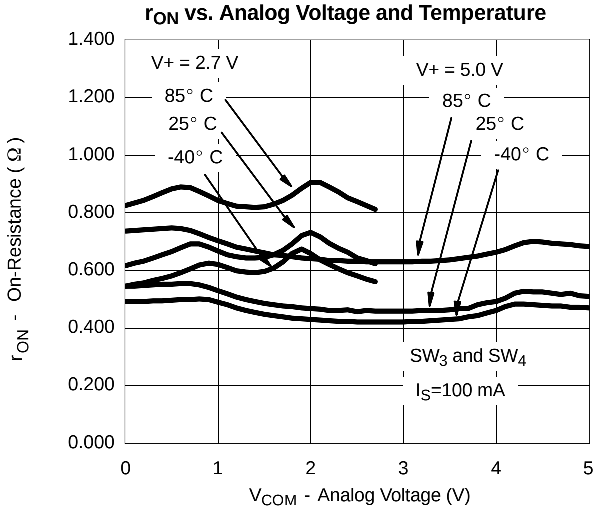
r_{ON} vs. V_{COM} and Single Supply Voltage



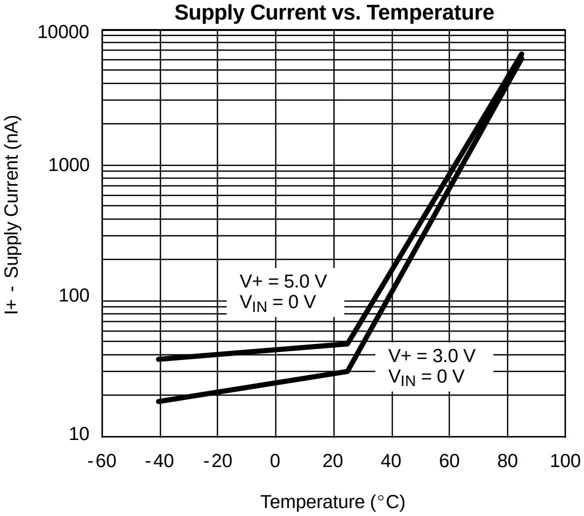
r_{ON} vs. Analog Voltage and Temperature



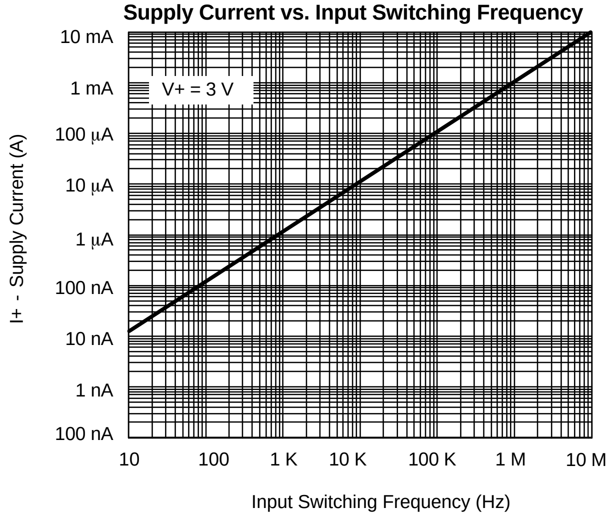
r_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

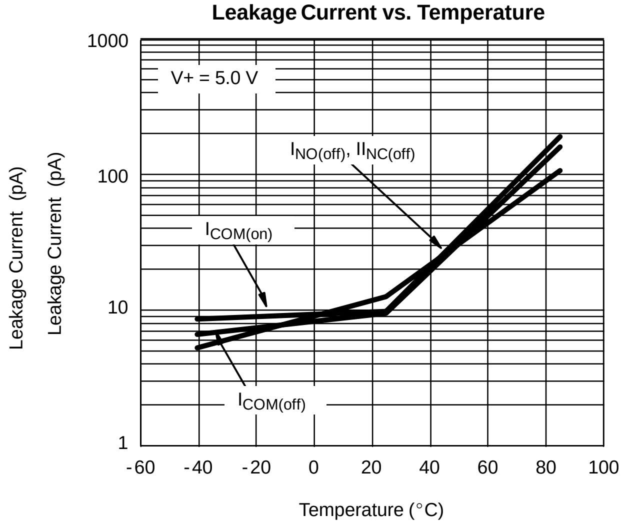


Supply Current vs. Input Switching Frequency

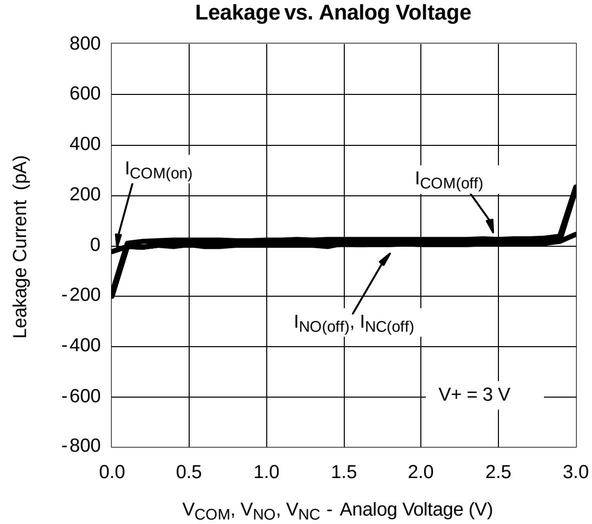


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

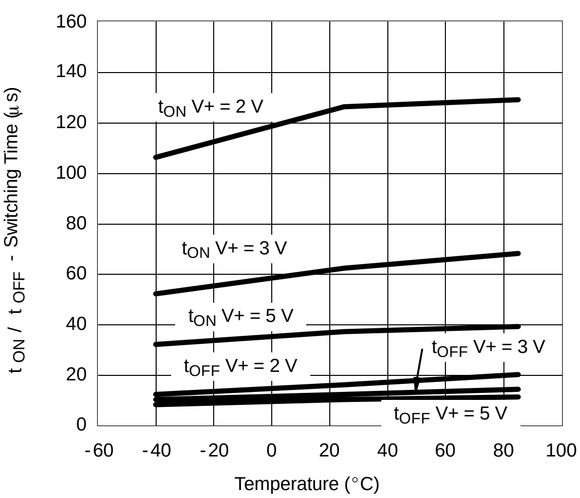
Leakage Current vs. Temperature



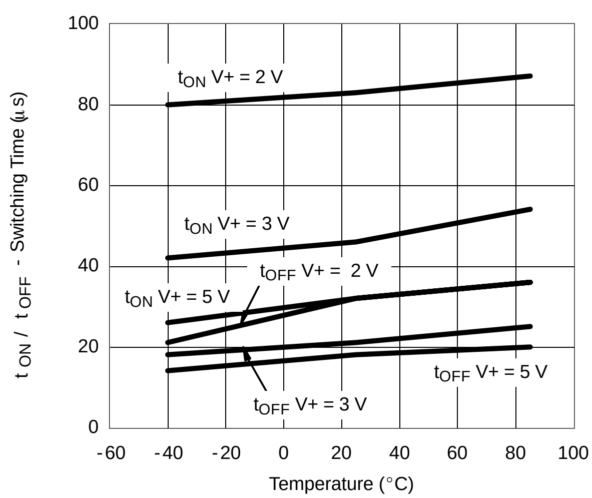
Leakage vs. Analog Voltage



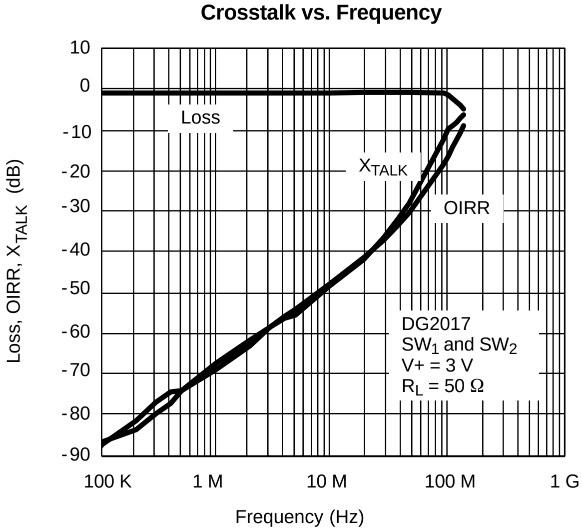
Switching Time vs. Temperature



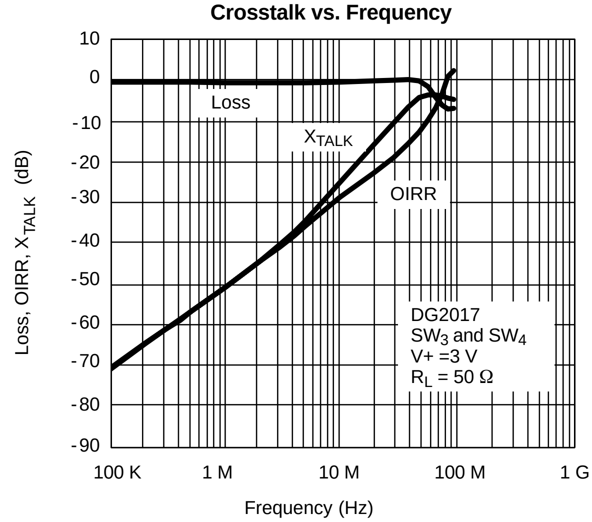
Switching Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

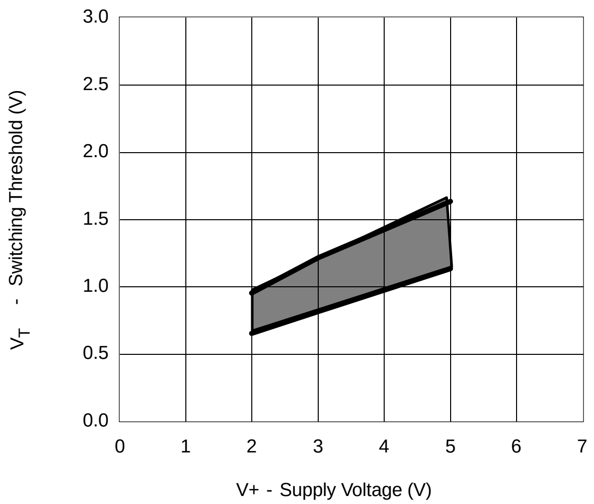


Insertion Loss, Off-Isolation Crosstalk vs. Frequency

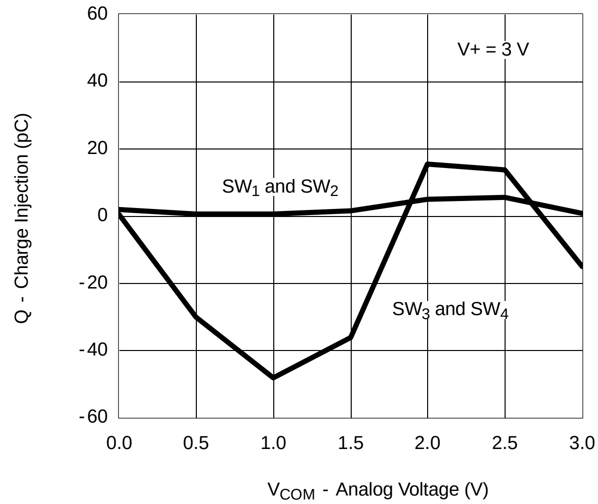


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage



TEST CIRCUITS

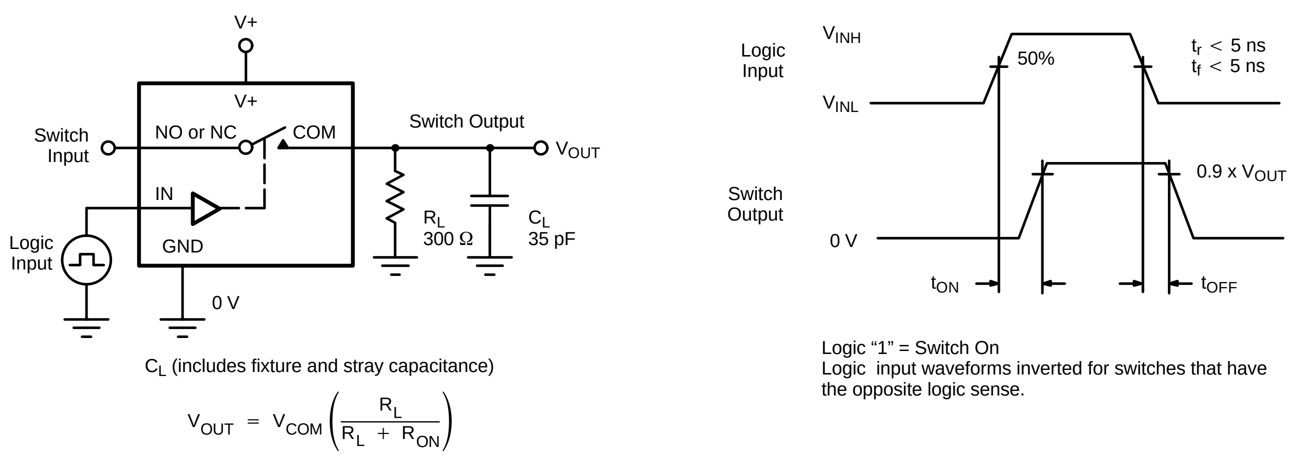
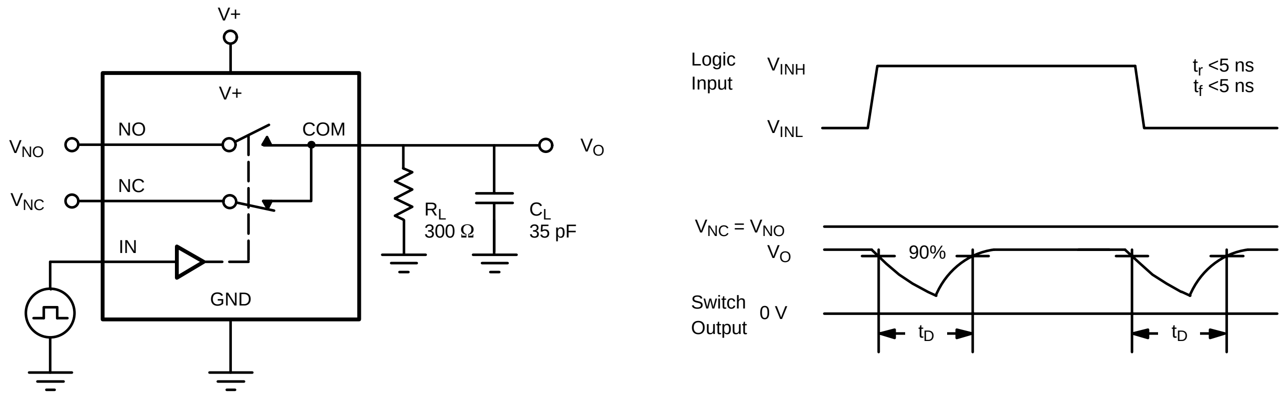


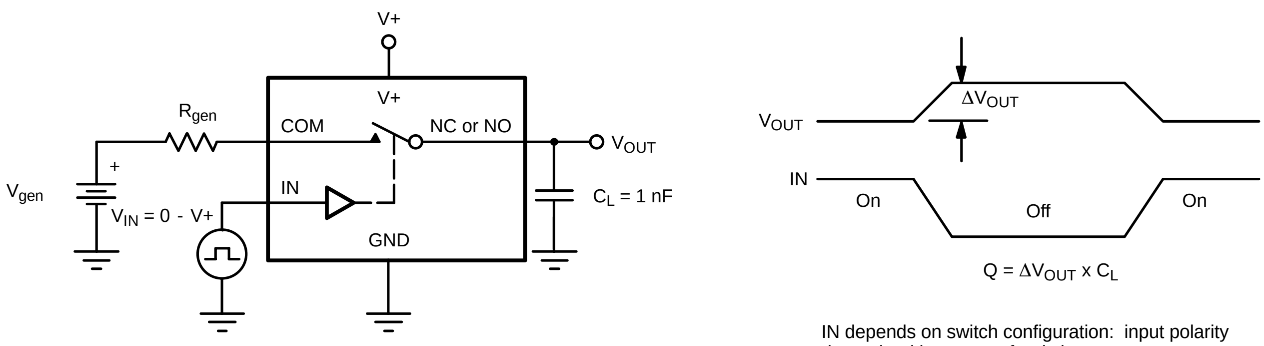
Figure 1. Switching Time

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

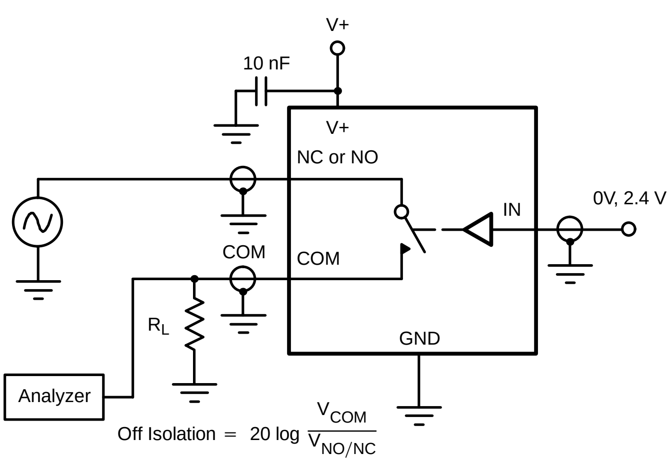


Figure 4. Off-Isolation

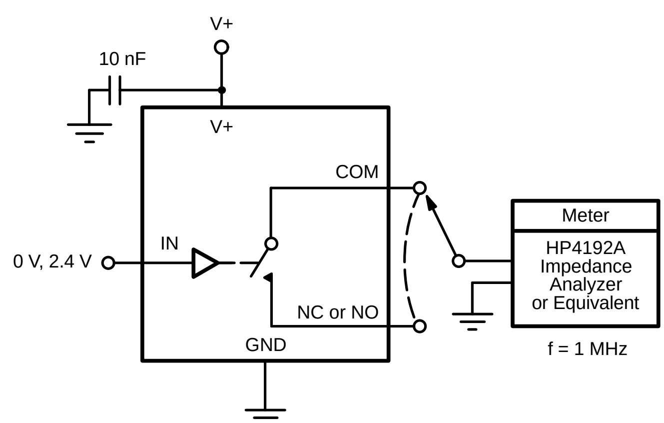


Figure 5. Channel Off/On Capacitance