



Low Voltage, Dual DPDT and Quad SPDT Analog Switches

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On Resistance
 - $r_{DS(on)}$: 6 Ω @ 2.7 V
- Low Voltage Logic Compatible
 - DG2019: $V_{INH} = 1$ V
- High Bandwidth: 150 MHz
- QFN-16 Package

BENEFITS

- Ideal for Both Analog and Digital Signal Switching
- Reduced Power Consumption
- High Accuracy
- Reduced PCB Space
- Fast Switching
- Low Leakage

APPLICATIONS

- Cellular Phones
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Portable Instrumentation

DESCRIPTION

The DG2018 and DG2019 are low voltage, single supply analog switches. The DG2018 is a dual double-pole/double-throw (DPDT) with two control inputs that each controls a pair of single-pole/double-throw (SPDT). The DG2019 uses one control pin to operate four independent SPDT switches.

When operated on a +3-V supply, the DG2018's control pins are compatible with 1.8-V digital logic. The DG2019 has an available feature of a V_L pin that allows a 1.0-V threshold for the control pin when V_L is powered with 1.5 V.

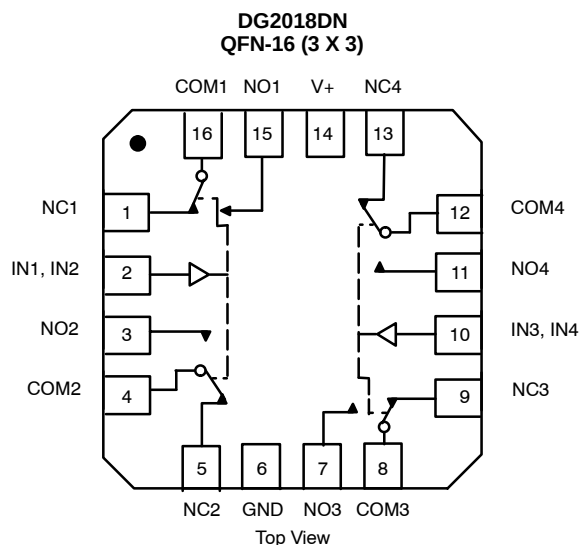
Built on Vishay Siliconix's low voltage submicron CMOS process, the DG2018 and DG2019 are ideal for high

performance switching of analog signals; providing low on-resistance (6 Ω @ +2.7 V), fast speed (T_{on} , T_{off} @ 42 ns and 16 ns), and a bandwidth that exceeds 150 MHz.

The DG2018 and DG2019 were designed to offer solutions that extend beyond audio/video functions, to providing the performance required for today's demanding mixed-signal switching in portable applications.

An epitaxial layer prevents latch-up. Brake-before-make is guaranteed for all SPDT's. All switches conduct equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



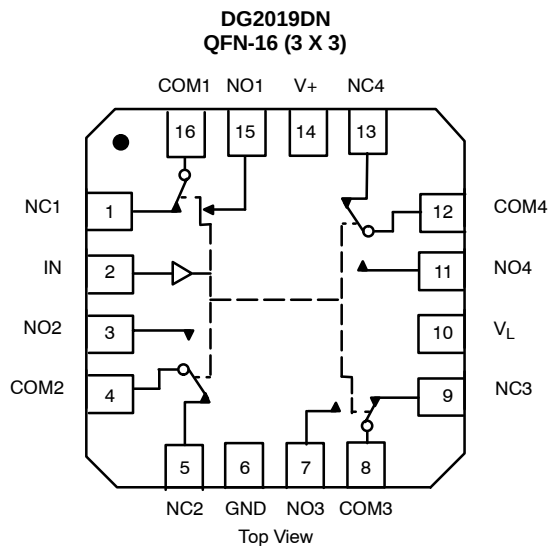
TRUTH TABLE

IN1, IN2		
Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

IN3, IN4		
Logic	NC3 and NC4	NO3 and NO4
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	QFN-16 (3 x 3 mm)	DG2018DN

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

TRUTH TABLE

Logic	NC1, 2, 3, and 4	NO1, 2, 3, and 4
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	QFN-16 (3 x 3 mm)	DG2019DN

ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+ -0.3 to +6 V

IN, COM, NC, NO -0.3 to (V+ + 0.3 V)

Continuous Current (Any terminal) ± 50 mA

Peak Current ± 100 mA
(Pulsed at 1 ms, 10% duty cycle)

Storage Temperature (D Suffix) -65 to 150°C

Power Dissipation (Packages)^b

QFN-16 (3 x 3 mm)^c 850 mW

Notes:

- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 4.0 mW/°C above 70°C



SPECIFICATIONS (V+ = 3 V)								
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10% (DG2018 Only) VIN = 0.5 or 1.4 V ^e (DG2019 Only) VL = 1.5 V, VIN = 0.4 or 1.0 V ^e		Temp ^a	Limits –40 to 85°C			Unit
					Min ^b	Typ ^c	Max ^b	
Analog Switch								
Analog Signal Range ^d	VNO, VNC, VCOM		Full	0		V+	V	
On-Resistance	rON	V+ = 2.7 V, VCOM = 0.2 V/1.5 V INO, INC = 10 mA	Room Full		6	12 15	Ω	
rON Flatness	rON Flatness	V+ = 2.7 V VCOM = 0 to V+, INO, INC = 10 mA	Room		0.5	2		
rON Match Between Channels	ΔrON		Room		0.6	3		
Switch Off Leakage Current	INO(off), INC(off)	V+ = 3.3 V, VNO, VNC =0.3 V/3 V VCOM = 3 V/ 0.3 V	Room Full	–1 –10	0.3	1 10	nA	
	ICOM(off)		Room Full	–1 –10	0.3	1 10		
Channel-On Leakage Current	ICOM(on)	V+ = 3.3 V, VNO, VNC = VCOM = 0.3 V/ 3 V	Room Full	–1 1.0	0.3	1 10		
Digital Control								
Input High Voltage	VINH		DG2018	Full	1.4		V	
		VL = 1.5 V	DG2019	Full	1.0			
Input Low Voltage	VINL		DG2018	Full		0.5		
		VL = 1.5 V	DG2019	Full		0.4		
Input Capacitance	Cin	f = 1 MHz	Full		9		pF	
Input Current	IINL or IINH	VIN = 0 or V+	Full	–1		1	μA	
Dynamic Characteristics								
Turn-On Time	tON	VNO or VNC = 2.0 V, RL = 300 Ω, CL = 35 pF	Room Full		42	55 65	ns	
Turn-Off Time	tOFF		Room Full		16	25 35		
Break-Before-Make Time	td	VNO or VNC = 2.0 V, RL = 50 Ω, CL = 35 pF	Full	1				
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω	Room		–1.46		pC	
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		–54		dB	
Crosstalk ^d	XTALK		Room		–53			
NO, NC Off Capacitance ^d	CNO(off)	VIN = 0 or V+, f = 1 MHz	Room		9		pF	
	CNC(off)		Room		9			
Channel-On Capacitance ^d	CNO(on)		Room		30			
	CNC(on)		Room		30			
Power Supply								
Power Supply Current	I+	VIN = 0 or V+	Full		0.01	1.0	μA	

Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.

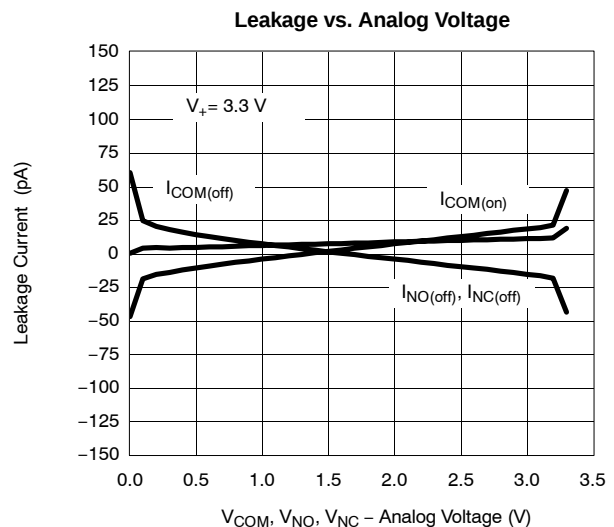
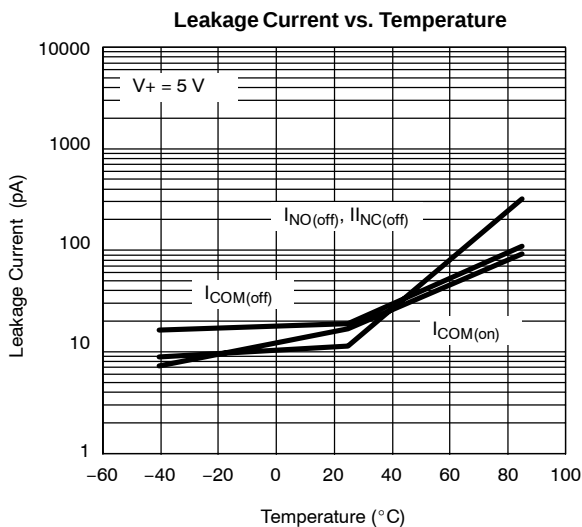
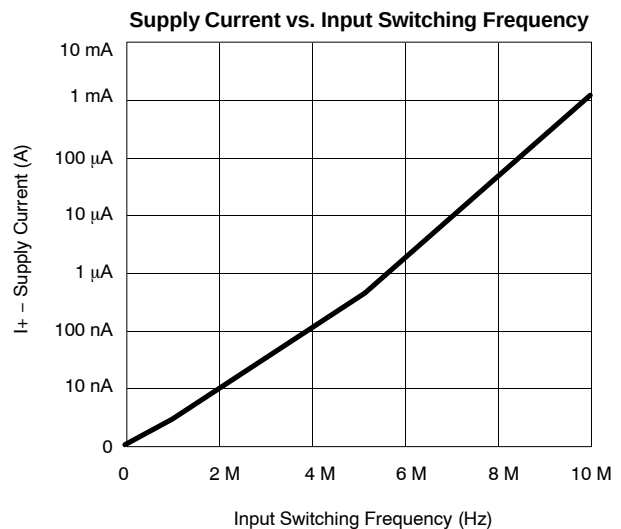
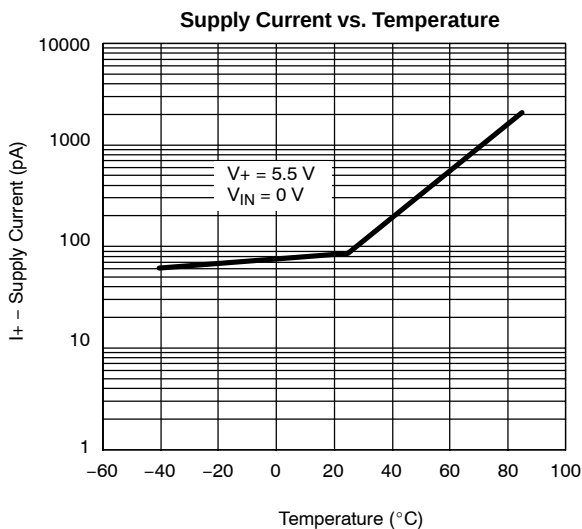
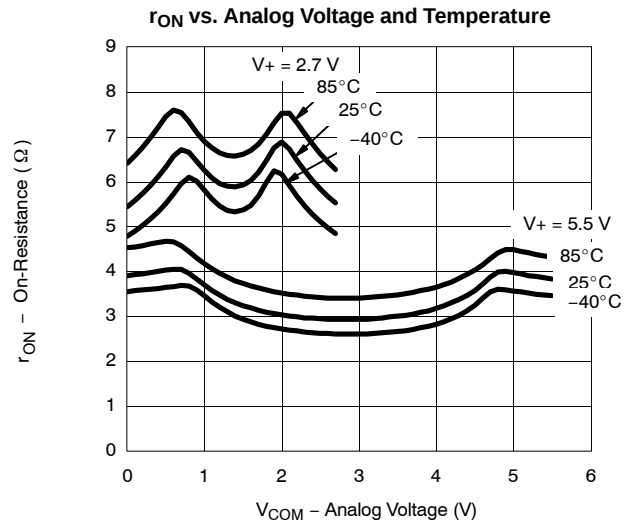
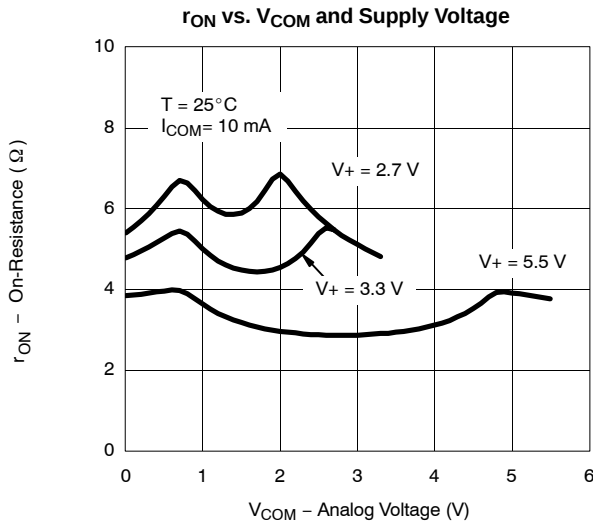
SPECIFICATIONS (V+ = 5 V)								
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10%, (DG2018 Only) VIN = 0.8 or 1.8 V ^e (DG2019 Only) VL = 1.5 V, VIN = 0.4 or 1.0 V ^e		Temp ^a	Limits –40 to 85°C			Unit
					Min ^b	Typ ^c	Max ^b	
Analog Switch								
Analog Signal Range ^d	VNO, VNC, VCOM			Full	0		V+	V
On-Resistance	rON	V+ = 4.5 V, VCOM = 3 V, INO, INC = 10 mA		Room Full		4	8 10	Ω
rON Flatness	rON Flatness	V+ = 4.5 V VCOM = 0 to V+, INO, INC = 10 mA		Room		0.6	1.2	
rON Match Between Channels	ΔrON			Room		0.6	1.2	
Switch Off Leakage Current ^f	INO(off), INC(off)	V+ = 5.5 V VNO, VNC = 1 V/4.5 V, VCOM = 4.5 V/1 V		Room Full	–1 –10	0.03	1 10	nA
	ICOM(off)			Room Full	–1 –10	0.03	1 10	
Channel-On Leakage Current ^f	ICOM(on)	V+ = 5.5 V, VNO, VNC = VCOM = 1 V/4.5 V		Room Full	–1 –10	0.03	1 10	
Digital Control								
Input High Voltage	VINH		DG2018	Full	1.8			V
		VL = 1.5 V	DG2019	Full	1.0			
Input Low Voltage	VINL		DG2018	Full			0.8	
		VL = 1.5 V	DG2019	Full			0.4	
Input Capacitance	Cin				Full	9		pF
Input Current	IINL or INIH	VIN = 0 or V+			Full	1	1	μA
Dynamic Characteristics								
Turn-On Time	tON	VNO or VNC = 3 V, RL = 300 Ω, CL = 35 pF			Room Full		44 52	ns
Turn-Off Time	tOFF				Room Full		19 33 35	
Break-Before-Make Time	td	VNO or VNC = 3 V, RL = 50 Ω, CL = 35 pF			Full	1		
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω			Room		–2.46	pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz			Room		–54	dB
Crosstalk ^d	XTALK				Room		–53	
Source-Off Capacitance ^d	CNO(off)	VIN = 0 or V+, f = 1 MHz			Room		7.5	pF
	CNC(off)				Room		7.5	
Channel-On Capacitance ^d	CNO(on)				Room		30	
	CNC(on)				Room		30	
Power Supply								
Power Supply Range	V+				1.8		5.5	V
Power Supply Current	I+	VIN = 0 or V+			Full		0.01 1.0	μA

Notes:

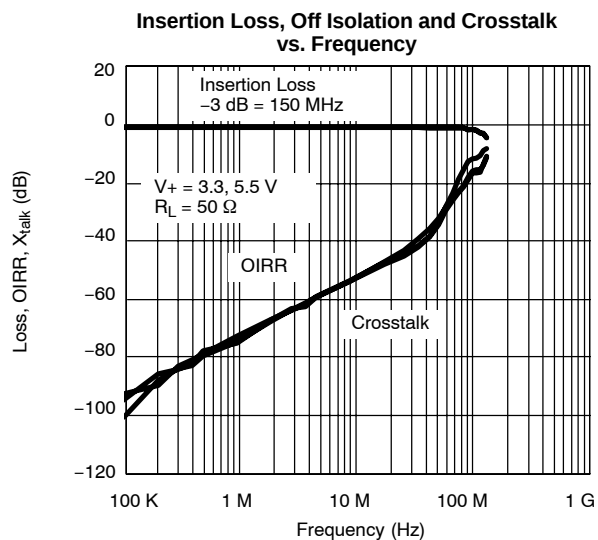
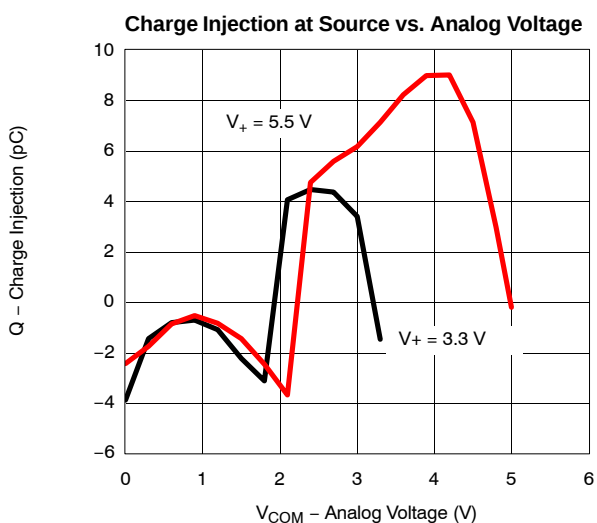
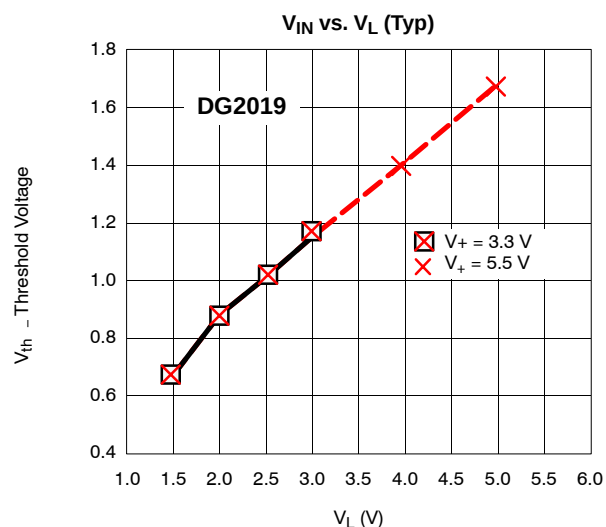
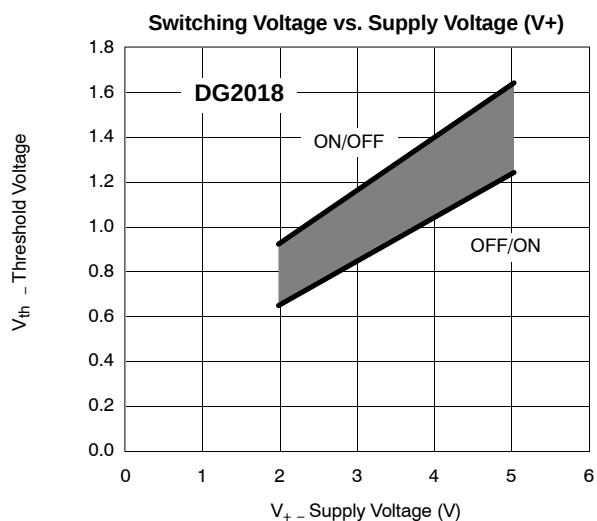
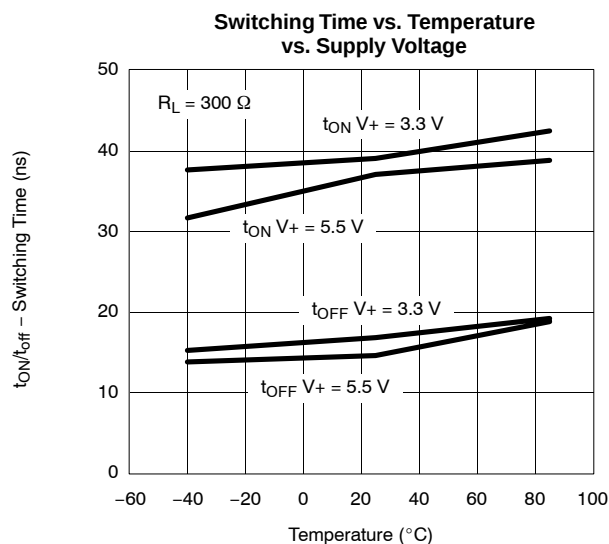
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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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TEST CIRCUITS

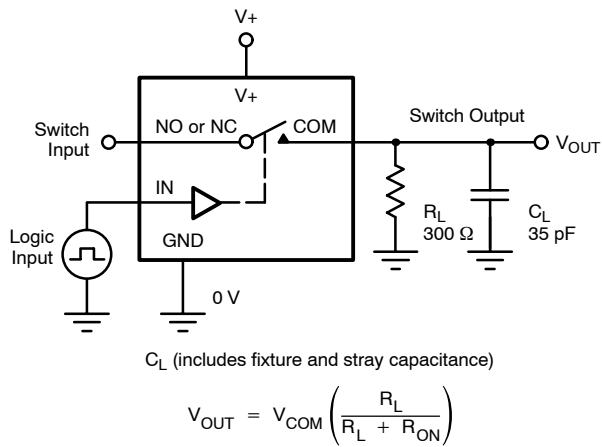


FIGURE 1. Switching Time

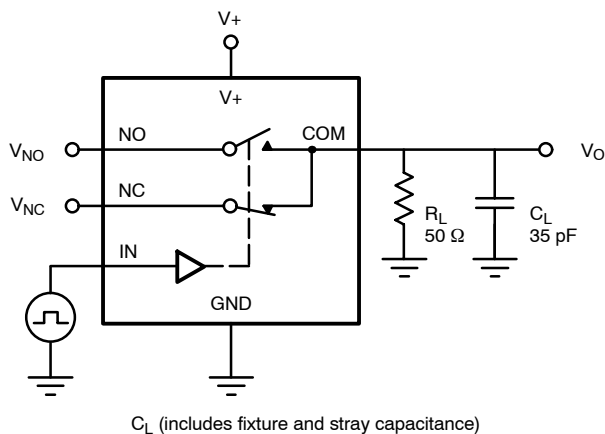
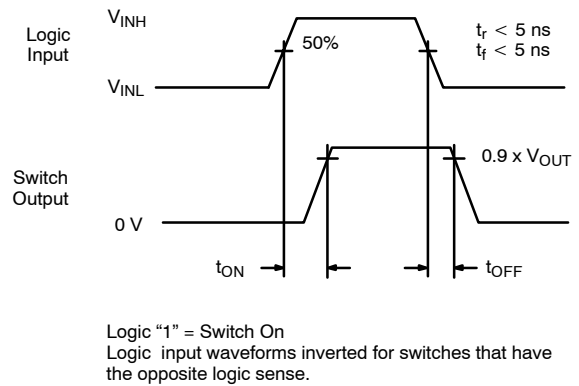


FIGURE 3. Break-Before-Make Interval

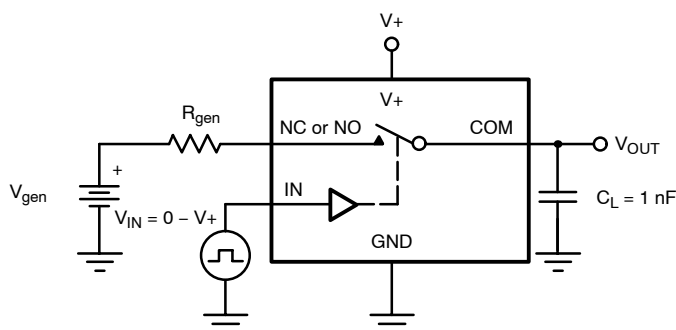
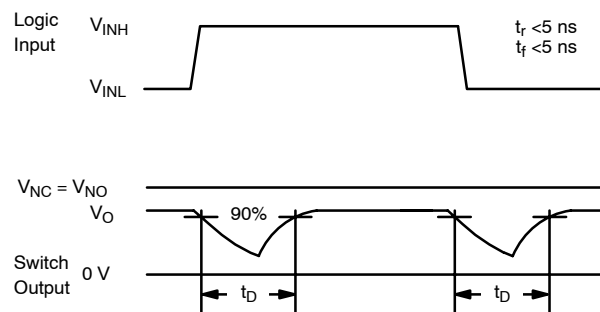
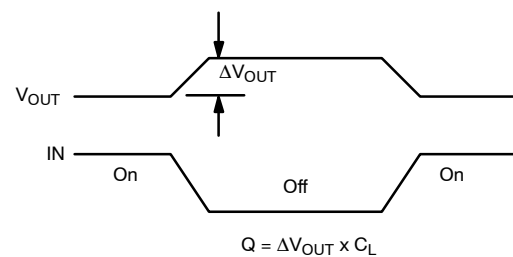


FIGURE 2. Charge Injection



IN depends on switch configuration: input polarity determined by sense of switch.

TEST CIRCUITS

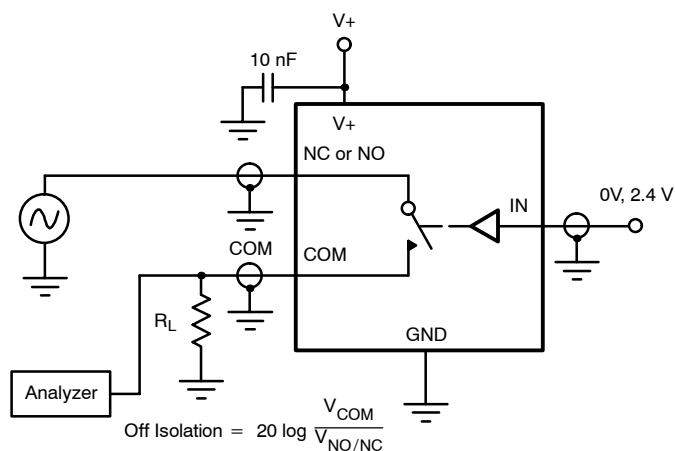


FIGURE 4. Off-Isolation

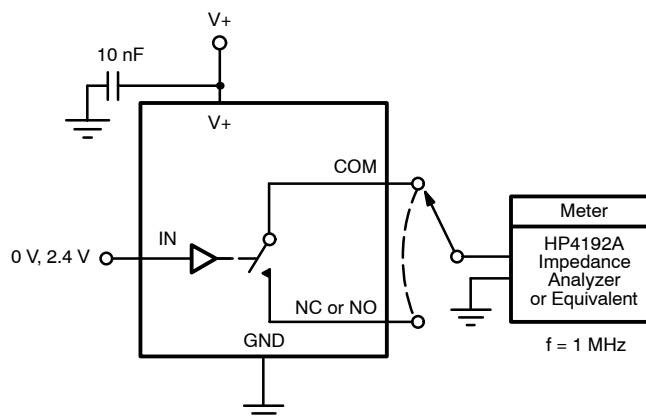


FIGURE 5. Channel Off/On Capacitance