



Low-Voltage Single SPDT Analog Switch

FEATURES

- Low Voltage Operation (1.6 V to 3.6 V)
- Low On-Resistance - $r_{DS(on)}$: 0.85 Ω Typ.
- Fast Switching - t_{ON} : 28 ns, t_{OFF} : 12 ns
- Low Leakage
- TTL/CMOS Compatible
- 6-Pin SC-70 Package

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits

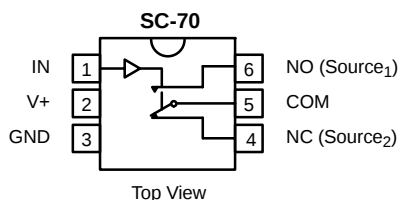
DESCRIPTION

The DG2714 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 28 ns, t_{OFF} : 12 ns), low on-resistance ($r_{DS(on)}$: 0.85 Ω) and small physical size (SC70), the DG2714 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2714 is built on Vishay Siliconix's low voltage submicron CMOS process. An epitaxial layer prevents latchup. Break-before -make is guaranteed for DG2714.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: E8xx

TRUTH TABLE

Logic	NC	NO
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	SC70-6	DG2714DL



ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	-0.3 to +4 V
IN, COM, NC, NO ^a	-0.3 to (V+ + 0.3 V)
Continuous Current (NO, NC and COM Pins)	±200 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	±300 mA
Storage Temperature (D Suffix)	-65 to 150°C

Power Dissipation (Packages)^b

6-Pin SO70 ^c	250 mW
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Notes:

- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 3.1 mW/°C above 70°C

SPECIFICATIONS (V+ = 1.8 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 1.8 V, ±10%, VIN = 0.4 or 1.1 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	VNO, VNC, VCOM		Full	0		V+	V
On-Resistance	rON	V+ = 1.8 V, VCOM = 0.2 V/0.9 V INO, INC = 10 mA	Room Full ^d		1.8	3.0 4.5	Ω
rON Flatness ^d	rON Flatness	V+ = 1.8 V, VCOM = 0 to V+, INO, INC = 10 mA	Room			2	
rON Match ^d	ΔrON		Room			0.06	
Switch Off Leakage Current ^f	INO(off), INC(off)	V+ = 2.2 V VNO, VNC = 0.2 V/2.0 V, VCOM = 2.0 V/0.2 V	Room Full ^d	-1 -10		1 10	nA
	ICOM(off)		Room Full ^d	-1 -10		1 10	
Channel-On Leakage Current ^f	ICOM(on)	V+ = 2.2 V, VNO, VNC = VCOM = 0.2 V/2.0 V	Room Full ^d	-1 -10		1 10	
Digital Control							
Input High Voltage	VINH		Full	1.1			V
Input Low Voltage	VINL		Full			0.4	
Input Capacitance ^d	Cin		Full		3.5		pF
Input Current ^f	IINL or IINH	VIN = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	tON	VNO or VNC = 1.5 V, RL = 300 Ω, CL = 35 pF Figures 1 and 2	Room Full ^d		55	75 89	ns
Turn-Off Time ^d	tOFF		Room Full ^d		19	39 40	
Break-Before-Make Time ^d	td		Room	3			
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω, Figure 3	Room		13		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		-64		dB
Crosstalk ^d	XTALK		Room		-64		
NO, NC Off Capacitance ^d	CNO(off), CNC(off)	VIN = 0 or V+, f = 1 MHz	Room		32		pF
Channel-On Capacitance ^d	CON		Room		78		

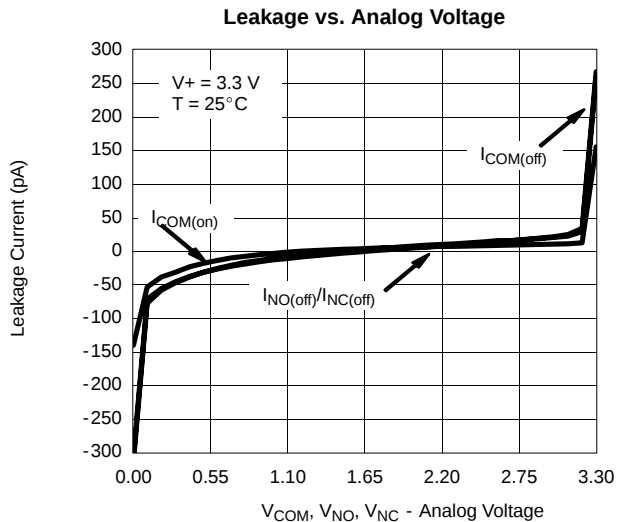
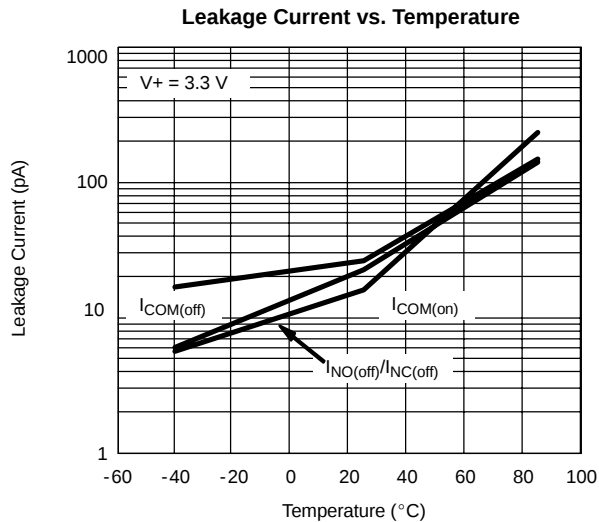
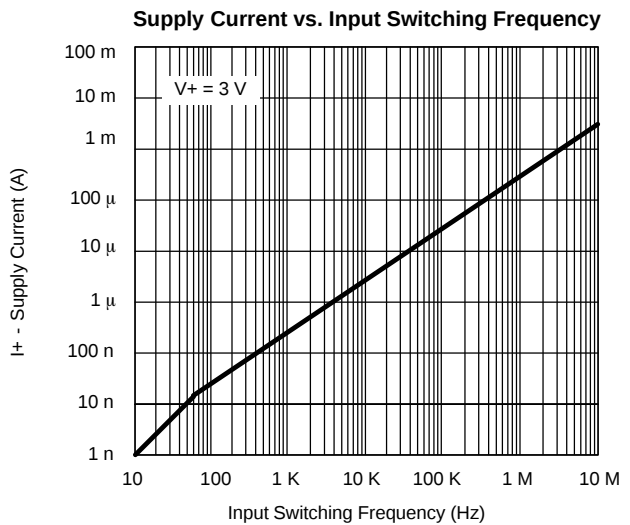
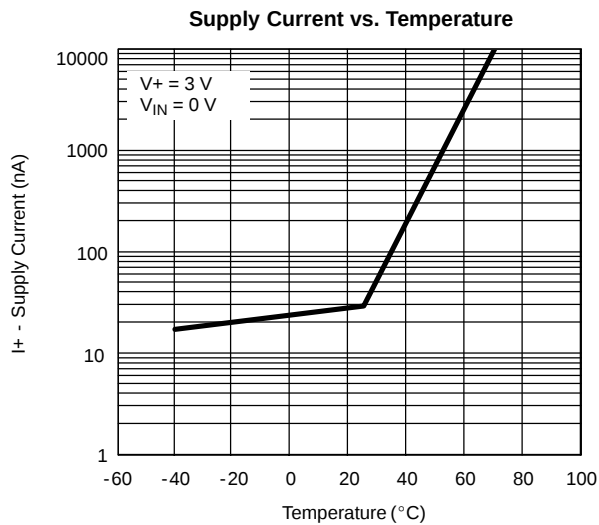
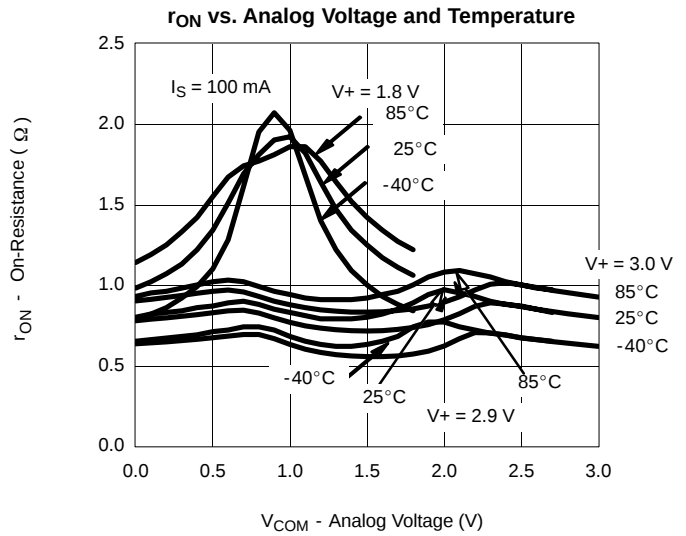
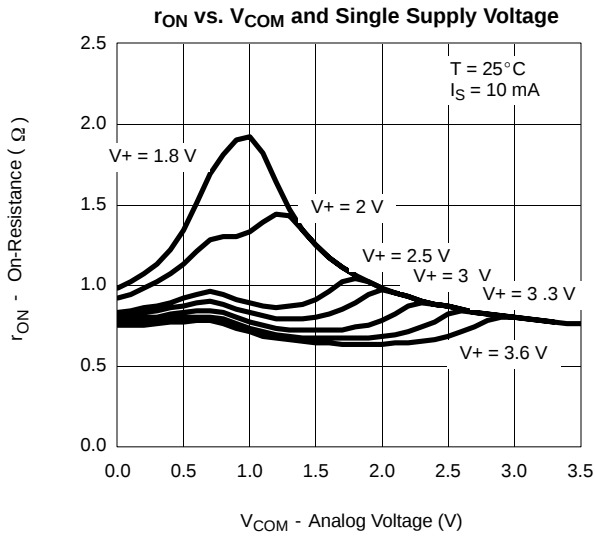
**SPECIFICATIONS (V+ = 3.0 V)**

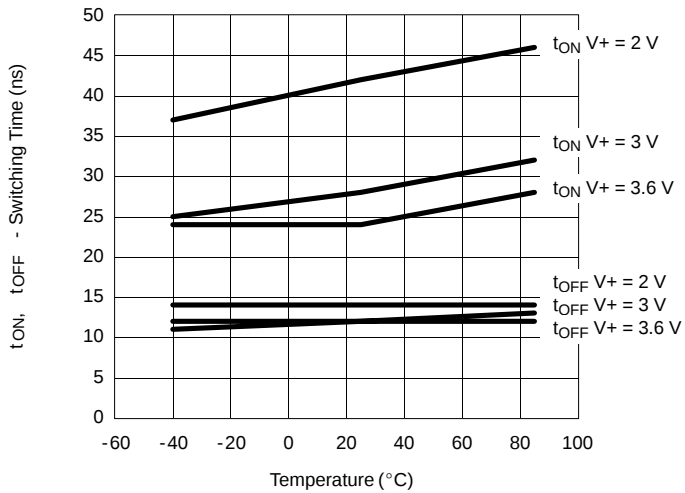
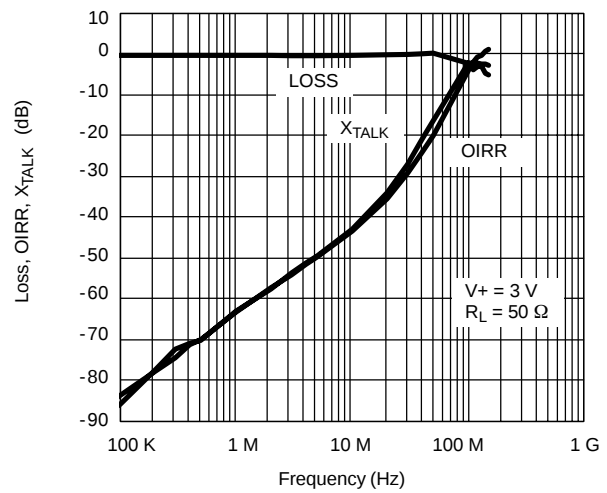
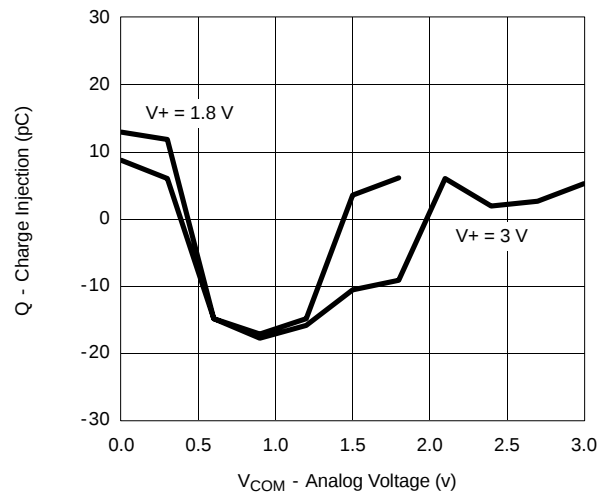
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, VIN = 0.5 or 1.5 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V, I _{NO} I _{NC} = 100 mA	Room Full		0.85	1.2 1.3	Ω
r _{ON} Flatness	r _{ON} Flatness	V+ = 2.7 V, V _{COM} = 0 to V+, I _{NO} , I _{NC} = 100 mA	Room			0.2	
r _{ON} MatchFlat	Δr _{ON}		Room			0.06	
Switch Off Leakage Current	I _{NO(off)} , I _{NC(off)}	V+ = 3.3 V V _{NO} , V _{NC} = 0.3 V/3 V, V _{COM} = 3 V/0.3 V	Room Full	-1 -10		1 10	nA
	I _{COM(off)}		Room Full	-1 -10		1 10	
Channel-On Leakage Current	I _{COM(on)}	V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 0.3 V/3 V	Room Full	-1 -10		1 10	
Digital Control							
Input High Voltage	V _{INH}		Full	1.5			V
Input Low Voltage	V _{INL}		Full			0.5	
Input Capacitance ^d	C _{in}		Full		3.3		pF
Input Current ^f	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 2.0 V, R _L = 300 Ω, C _L = 35 pF Figure 1 and 2	Room Full		28	51 55	ns
Turn-Off Time	t _{OFF}		Room Full		12	33 34	
Break-Before-Make Time	t _d		Room	1			
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		9		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-64		dB
Crosstalk ^d	X _{TALK}		Room		-64		
NO, NC Off Capacitance ^d	C _{NO(off)} , C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		30		pF
Channel-On Capacitance ^d	C _{ON}		Room		77		
Power Supply							
Power Supply Range	V+			1.5		3.6	V
Power Supply Current	I+	V+ = 3.6 V, V _{IN} = 0 or V+			0.01	1.0	μA

Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by 3-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)****Switching Time vs. Temperature and Supply Voltage****Insertion Loss, Off-Isolation, Crosstalk vs. Frequency****Charge Injection vs. Analog Voltage**

TEST CIRCUITS

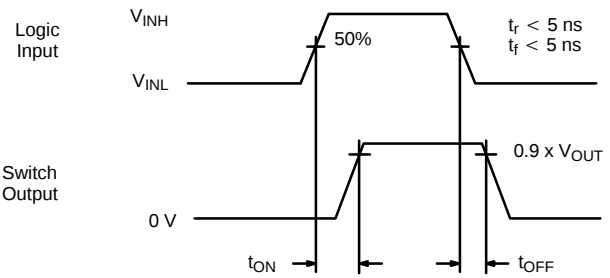
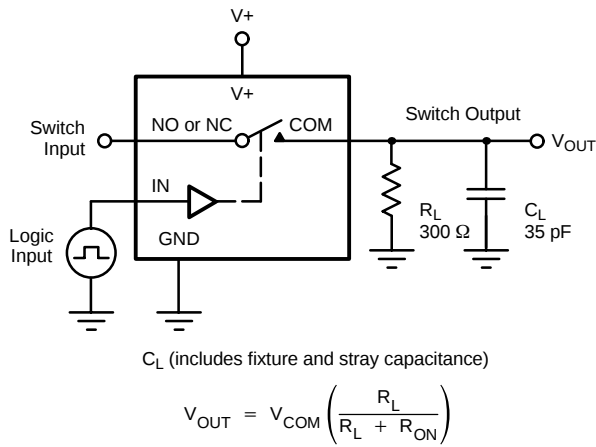


FIGURE 1. Switching Time

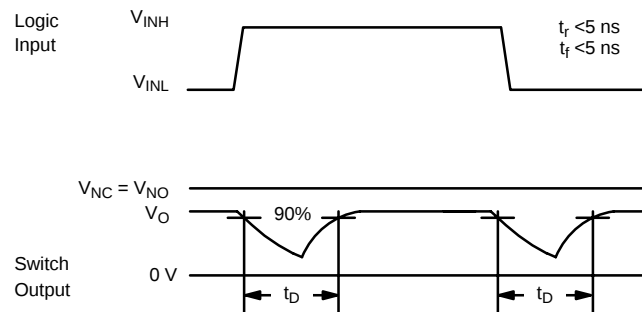
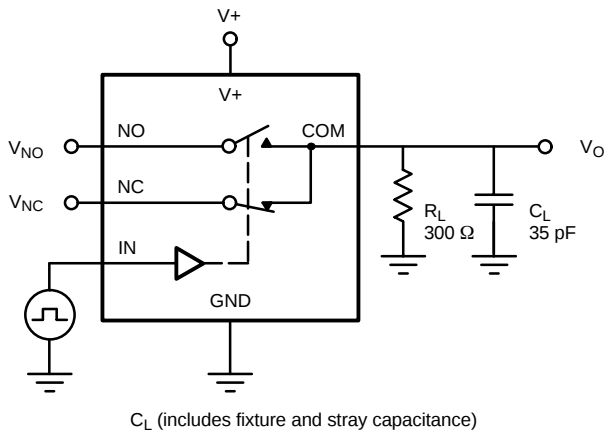
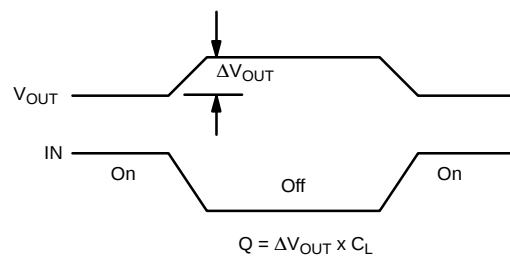
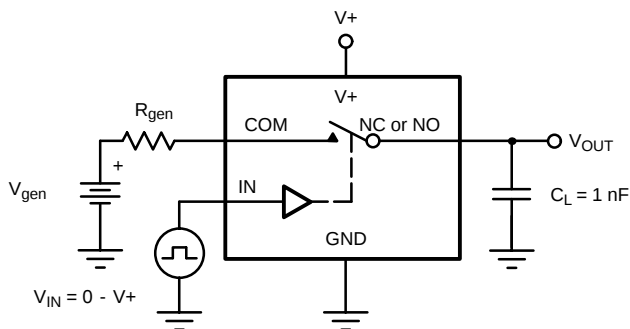


FIGURE 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

TEST CIRCUITS

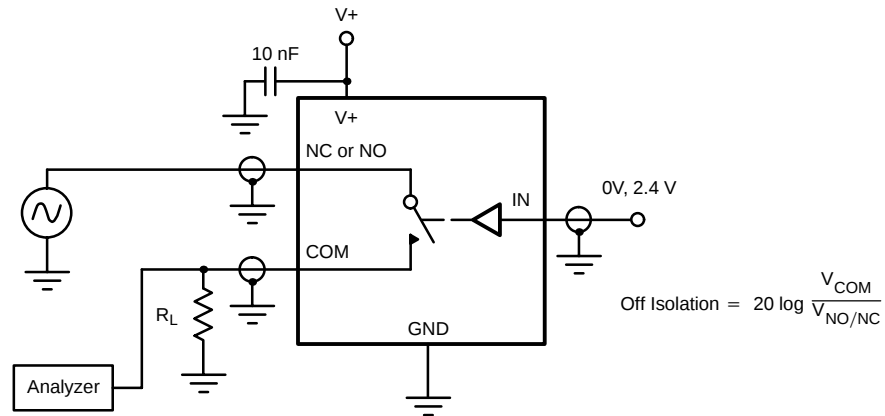


FIGURE 4. Off-Isolation

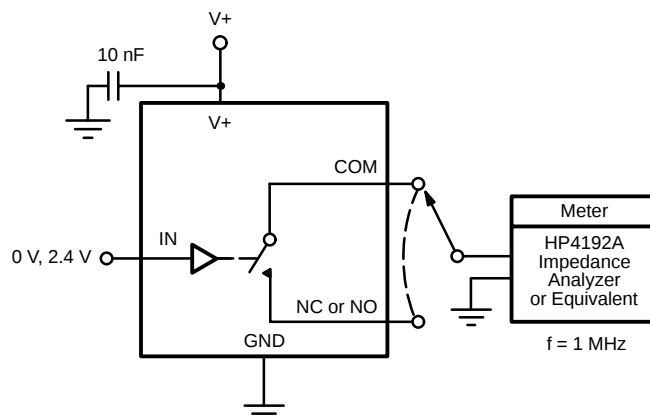


FIGURE 5. Channel Off/On Capacitance