Improved Quad SPST CMOS Analog Switches

FEATURES

- Low On-Resistance: 45 Ω
- Low Power Consumption: 1.0 mW
- Fast Switching Action—t_{ON}: 120 ns
- Low Charge Injection
- TTL/CMOS Logic Compatible

BENEFITS

- Low Signal Errors and Distortion
- Reduced Power Supply Consumption
- Faster Throughput
- Reduced Pedestal Errors
- Simple Interfacing

APPLICATIONS

- Audio Switching
- Data Acquisition
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Medical Instruments

DESCRIPTION

The DG444B/445B are monolithic quad analog switches designed to provide high speed, low error switching of analog and audio signals. The DG444B/445B are upgrades to the original DG444/445.

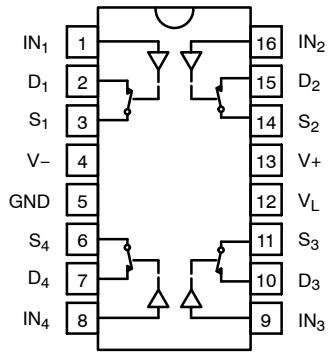
Combing low on-resistance (45 Ω, typ.) with high speed (t_{ON} 120 ns, typ.), the DG444B/445B are ideally suited for Data Acquisition, Communication Systems, Automatic Test Equipment, or Medical Instrumentation. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

The DG444B/445B are built using Vishay Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

When on, each switch conducts equally well in both directions and blocks input voltages to the supply levels when off.

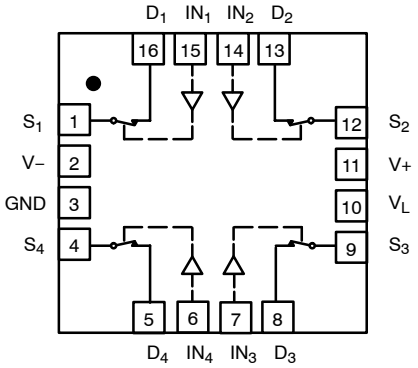
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG444B
Dual-In-Line and SOIC



Top View

DG444B
QFN16 (4x4 mm)



Top View

TRUTH TABLE		
Logic	**DG444B**	**DG445B**
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
–40 to 85°C	16-Pin Plastic DIP	DG444BDJ
		DG445BDJ
	16-Pin Narrow SOIC	DG444BDY
		DG445BDY
	16-Pin QFN 4x4 mm	DG444BDN
		DG445BDN

ABSOLUTE MAXIMUM RATINGS

V+ to V– . . . . . 44 V
GND to V– . . . . . 25 V
V_L . . . . . (GND –0.3 V) to (V+) + 0.3 V
Digital Inputs[a] V_S, V_D . . . . . (V–) –2 V to (V+) +2 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) . . . . . 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) . . . . . 100 mA
Storage Temperature . . . . . –65 to 125°C

Power Dissipation (Package)b
16-Pin Plastic DIP[c] . . . . . 470 mW
16-Pin Narrow Body SOIC[d] . . . . . 640 mW
QFN-16 . . . . . 850 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 8 mW/°C above 75°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS FOR DUAL SUPPLIES

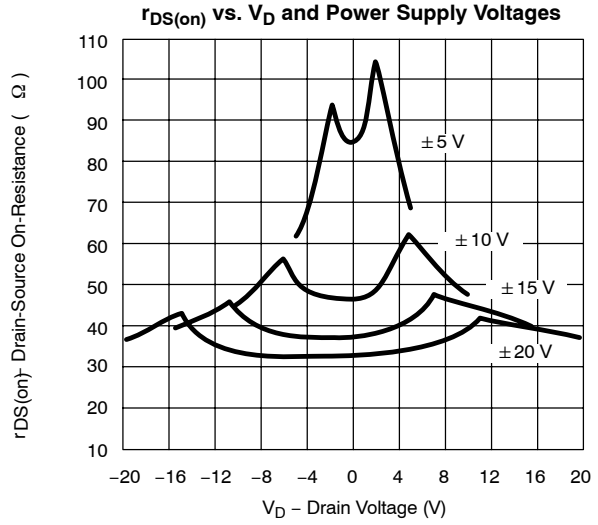
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = 1 mA, V_D = ∓10 V	Room Full		45	80 95	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_D = ∓14 V, V_S = ∓14 V	Room Full	–0.5 –5	±0.01	0.5 5	nA
	$I_{D(off)}$		Room Full	–0.5 –5	±0.01	0.5 5	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = ∓14 V	Room Full	–0.5 –10	∓0.02	0.5 10	
Digital Control							
Input Voltage Low	V_{INL}		Full			0.8	V
Input Voltage High	V_{INH}		Full	2.4			
Input Current V_{IN} Low	I_{INL}	V_{IN} under test = 0.8 V, All Other = 2.4 V	Full	–1	–0.01	1	µA
Input Current V_{IN} High	I_{INH}	V_{IN} under test = 2.4 V, All Other = 0.8 V	Full	–1	0.01	1	
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF V_S = ±10 V, See Figure 2	Room			300	ns
Turn-Off Time	t_{OFF}		Room			200	
Charge Injection[e]	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω	Room		1		pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 15 pF, V_S = 1 V_{RMS} f = 100 kHz	Room		90		dB
Crosstalk (Channel-to-Channel)[d]	X_{TALK}		Room		95		
Source Off Capacitance	$C_{S(off)}$	V_S = 0 V, f = 100 kHz	Room		5		pF
Drain Off Capacitance	$C_{D(off)}$		Room		5		
Channel On Capacitance	$C_{D(on)}$	V_S V_D = 0 V, f = 1 MHz	Room		16		
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full			1 5	µA
Negative Supply Current	I–		Room Full	–1 –5			
Logic Supply Current	I_{IN}		Room Full			1 5	

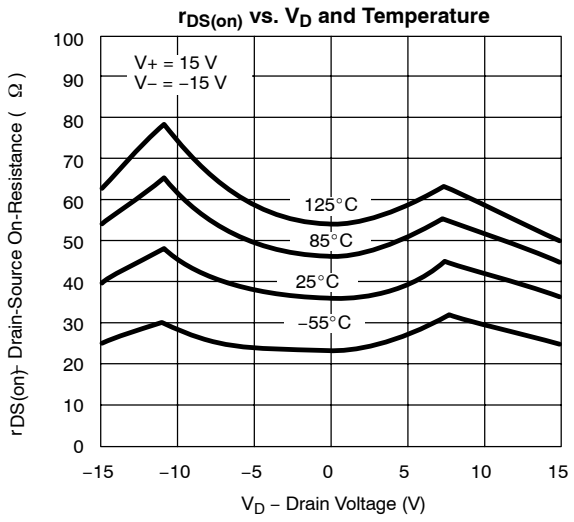
SPECIFICATIONS FOR UNIPOLAR SUPPLIES

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V– = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix –40 to 85°C			Unit
				Min[b]	Typ[c]	Max[b]	
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		12	V
Drain-Source On-Resistance[d]	$r_{DS(on)}$	I_S = 1 mA, V_D = 3 V, 8 V	Room Full		90	160 200	Ω
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, V_S = 8 V See Figure 2	Room		120	300	ns
Turn-Off Time	t_{OFF}		Room		60	200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room		4		pC
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full			1 5	µA
Negative Supply Current	I–		Room Full	–1 –5			
Logic Supply Current	I_{IN}	V_L = 5.25 V, V_{IN} = 0 or 5 V	Room Full			1 5	

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

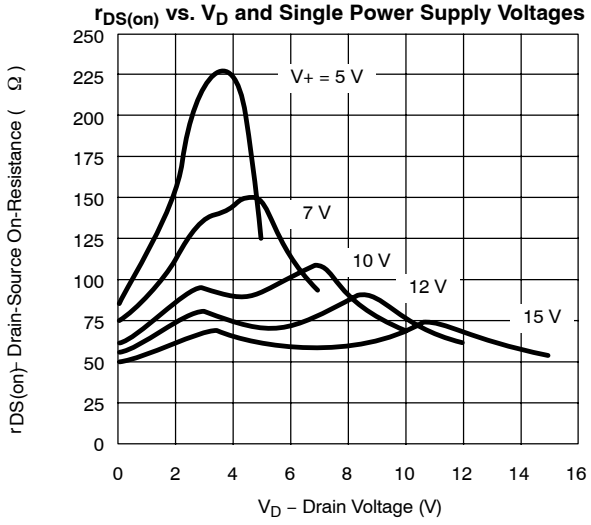
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



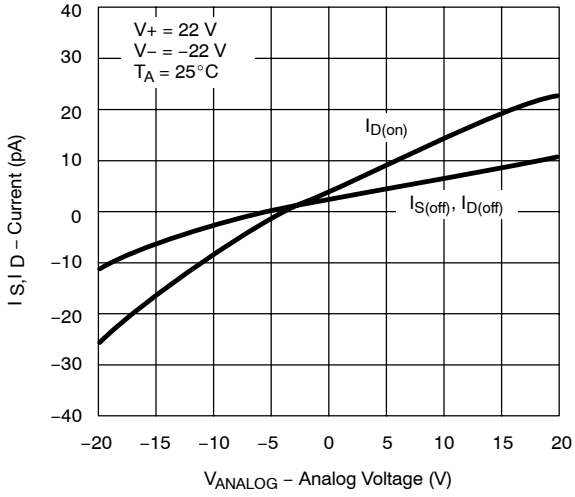


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

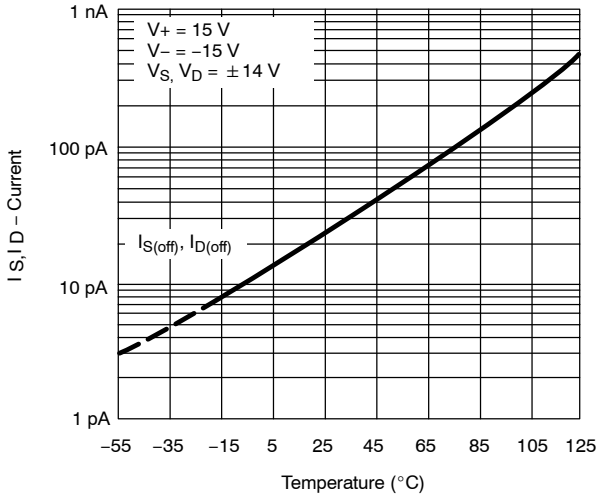
$r_{DS(on)}$ vs. V_D and Single Power Supply Voltages



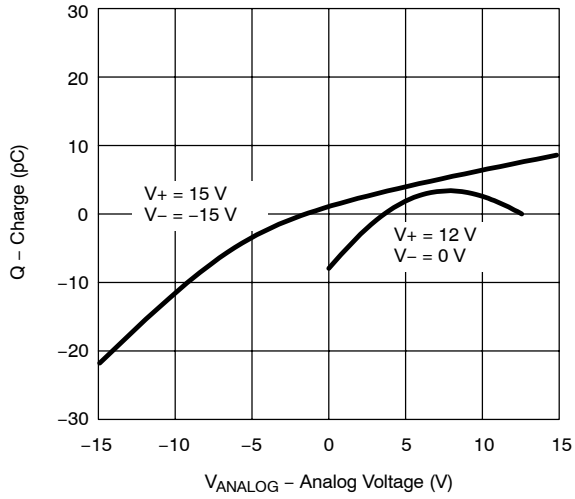
Leakage Currents vs. Analog Voltage



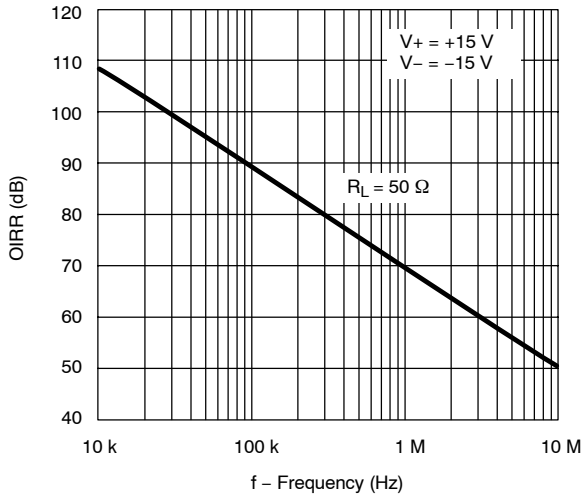
Leakage Current vs. Temperature



Q_S, Q_D – Charge Injection vs. Analog Voltage



Off Isolation vs. Frequency



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

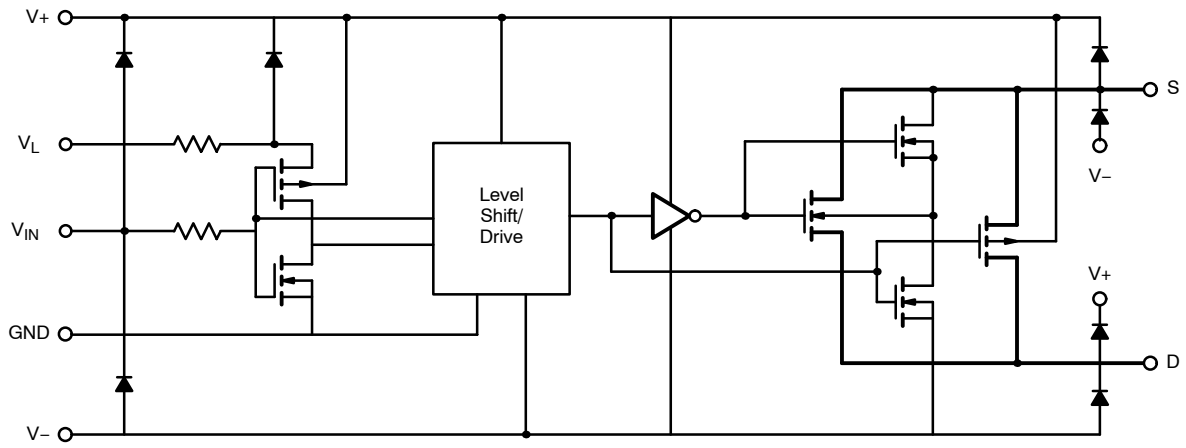
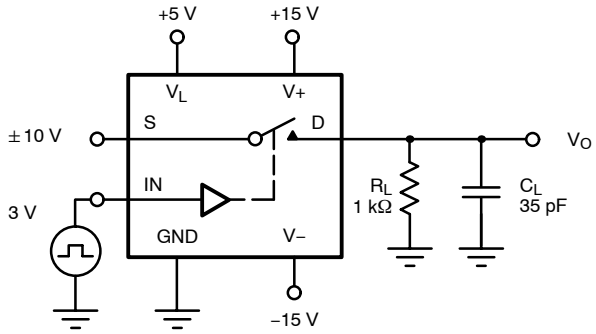
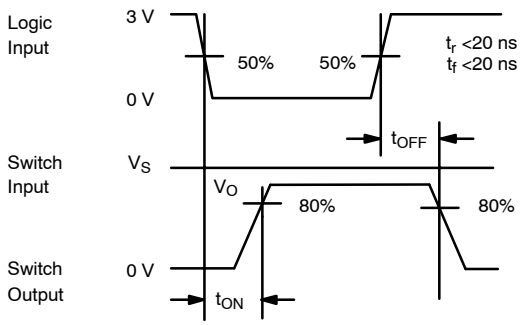


FIGURE 1.

TEST CIRCUITS



C_L (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG445.

FIGURE 2. Switching Time

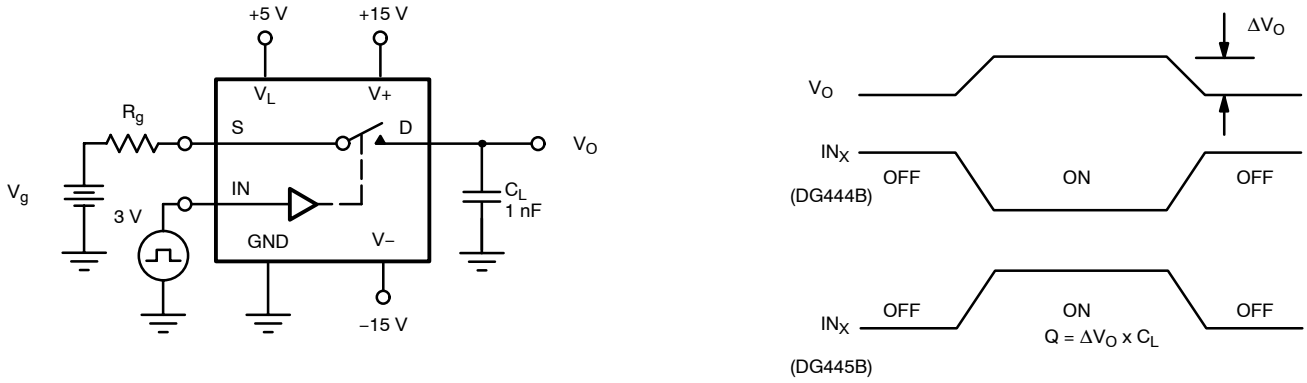
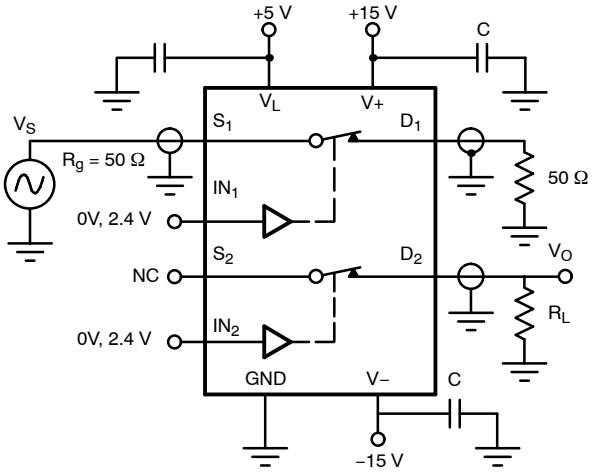


FIGURE 3. Charge Injection

TEST CIRCUITS

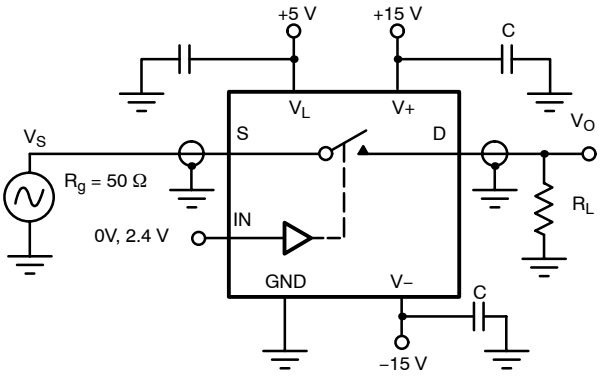
C = 1 mF tantalum in parallel with 0.01 mF ceramic



X_{TALK} Isolation = 20 log $\left|\frac{V_S}{V_O}\right|$

C = RF bypass

FIGURE 4. Crosstalk



Off Isolation = 20 log $\left|\frac{V_S}{V_O}\right|$

FIGURE 5. Off Isolation

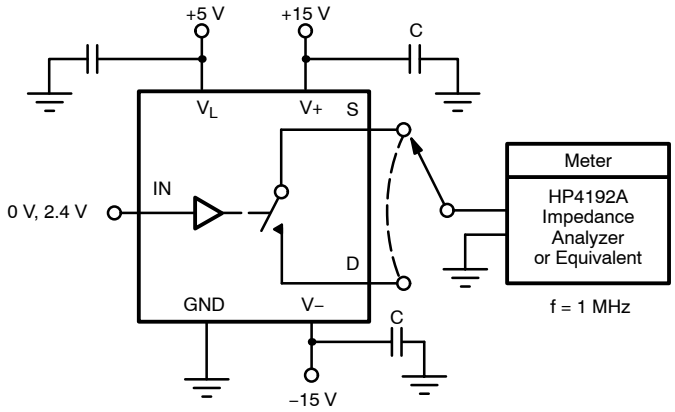


FIGURE 6. Source/Drain Capacitances

APPLICATIONS

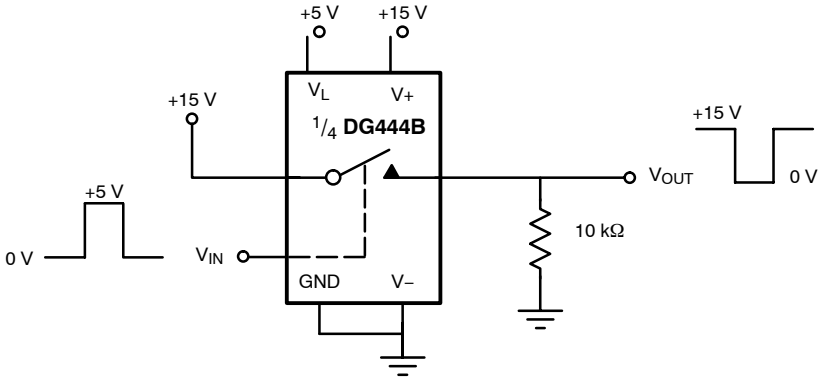


FIGURE 7. Level Shifter

Document Number: 72626
S-32554—Rev. A, 15-Dec-03

APPLICATIONS

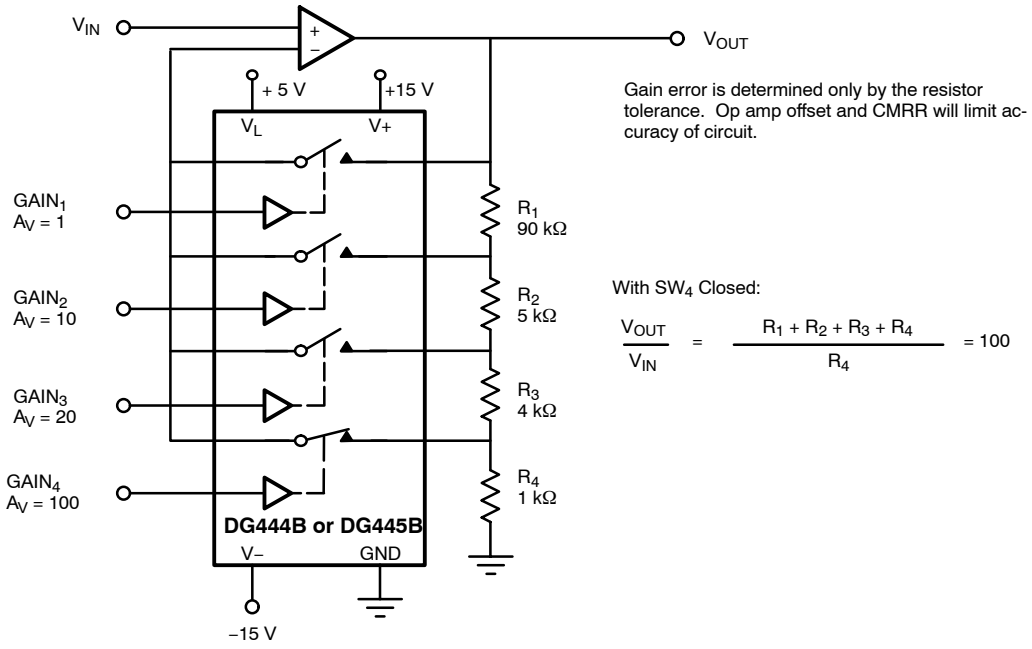


FIGURE 8. Precision-Weighted Resistor Programmable-Gain Amplifier

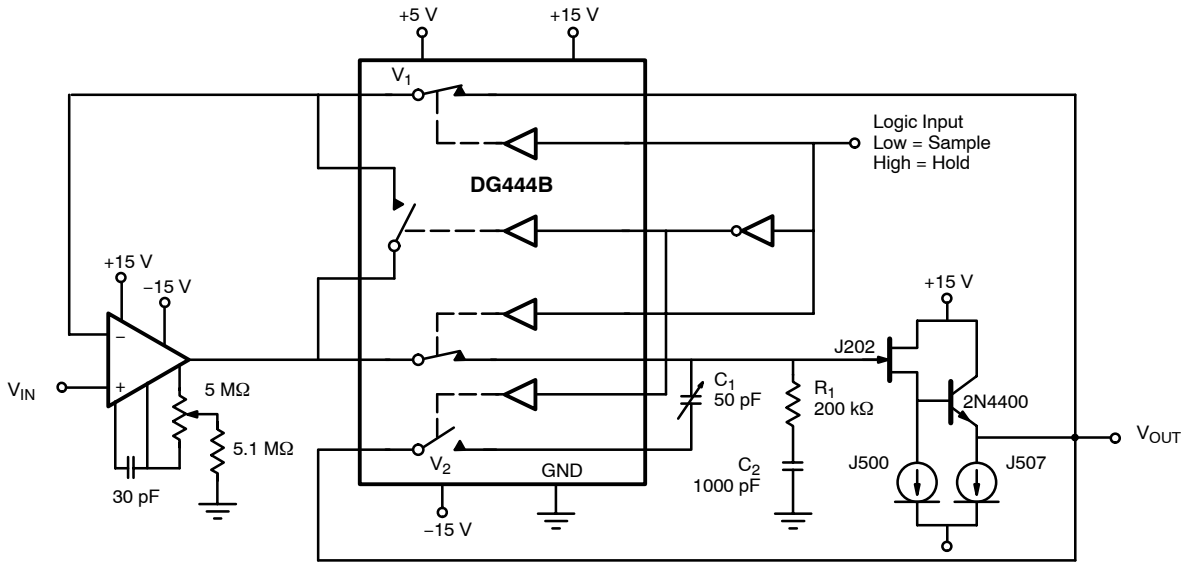


FIGURE 9. Precision Sample-and-Hold