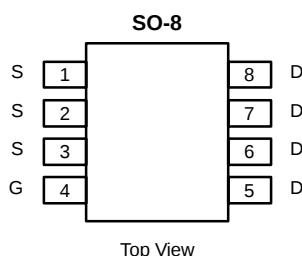




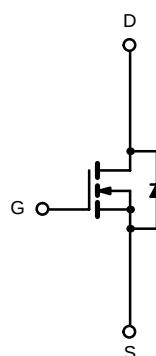
N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.024 @ $V_{GS} = 10$ V	7.5
	0.03 @ $V_{GS} = 6.0$ V	6.5



Ordering Information: Si4450DY
Si4450DY-T1 (with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	7.5	A
		5.5	
Pulsed Drain Current	I_{DM}	50	
Continuous Source Current (Diode Conduction) ^a	I_S	2.1	
Maximum Power Dissipation ^a	P_D	2.5	W
		1.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

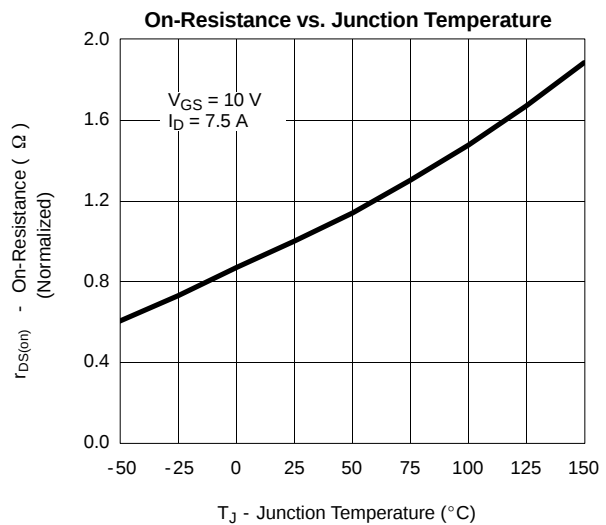
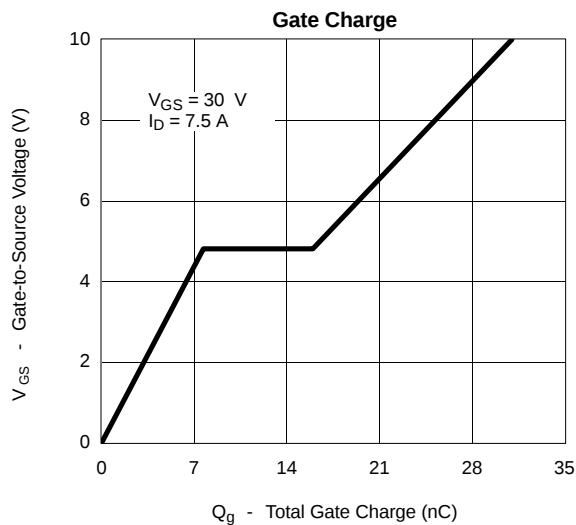
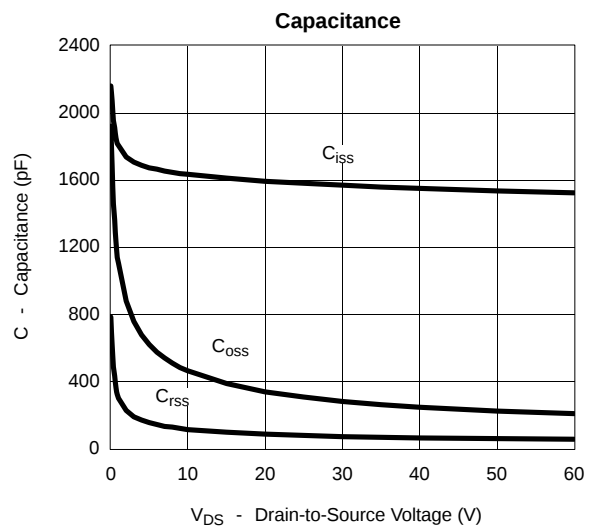
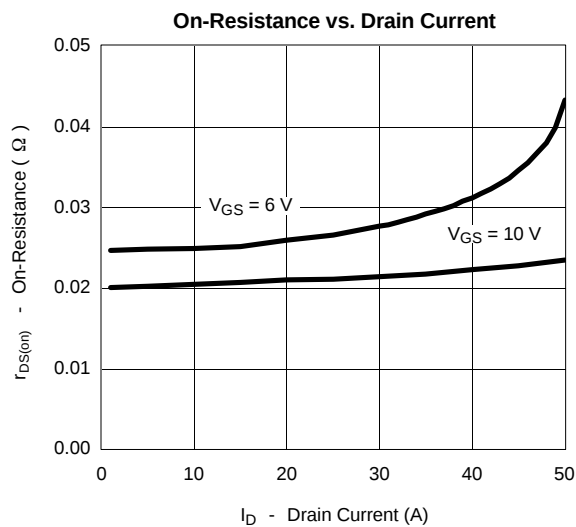
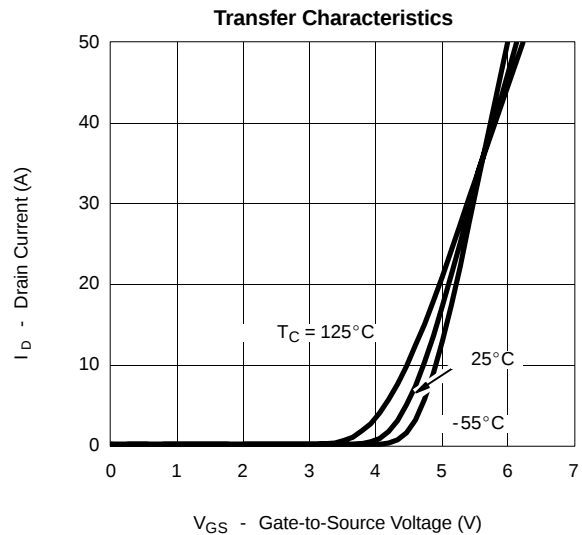
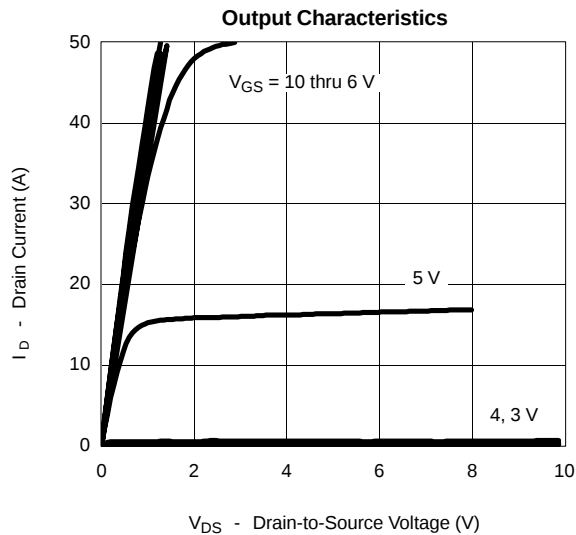
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			20	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 7.5\ \text{A}$		0.020	0.024	Ω
		$V_{GS} = 6.0\ \text{V}$, $I_D = 6.5\ \text{A}$		0.025	0.03	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 7.5\ \text{A}$		18.5		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.1\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.75	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = 30\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 7.5\ \text{A}$		31	50	nC
Gate-Source Charge	Q_{gs}			7.7		
Gate-Drain Charge	Q_{gd}			8.3		
Gate Resistance	R_g		1		5.8	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\ \text{V}$, $R_L = 30\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		16	30	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			41	80	
Fall Time	t_f			21	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		46	80	

Notes

- a. For design aid only; not subject to production testing.
b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

