

Dual N-Channel 50-V (D-S) Dual MOSFET

CHARACTERISTICS

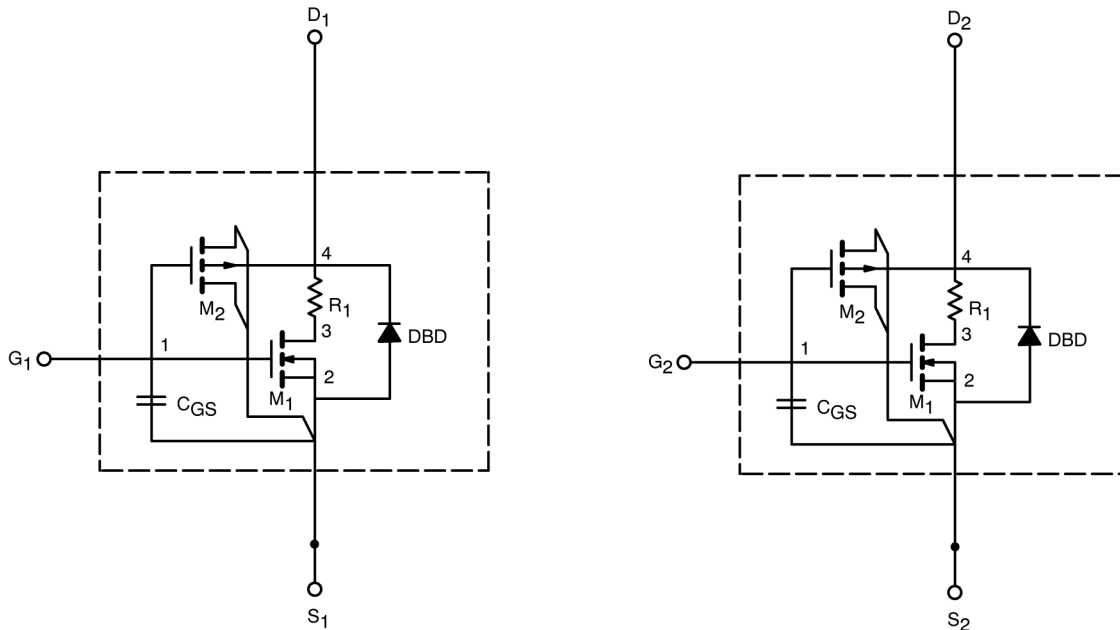
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model schematic is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model Si4649EY

Vishay Siliconix



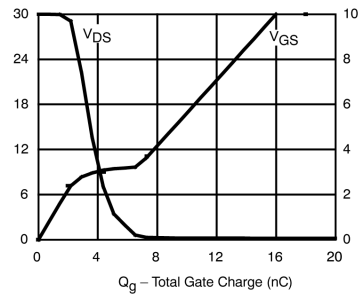
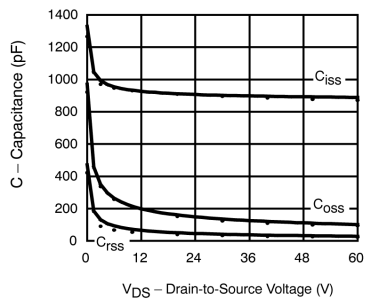
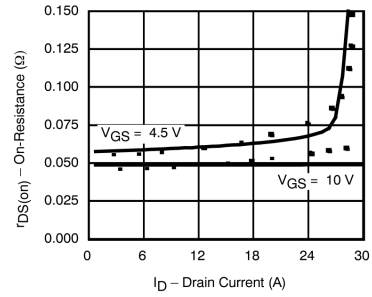
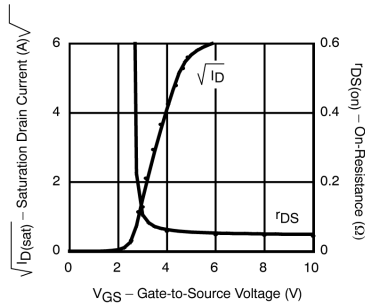
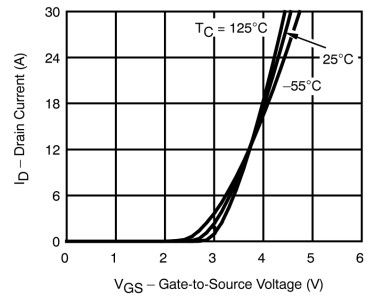
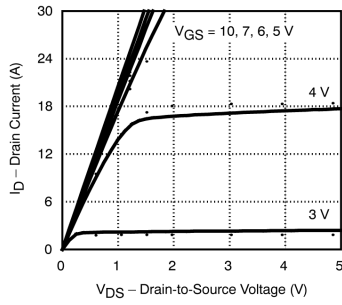
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Condition	Measured Data	Unit
Static				
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.75	V
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	100	A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10V, I _D = 4.5 A	0.048	Ω
		V _{GS} = 4.5V, I _D = 3.9 A	0.058	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 4.5 A	13	S
Diode Forward Voltage ^a	V _{SD}	I _S = 2 A, V _{GS} = 0 V	0.81	V
Dynamic^b				
Total Gate Charge ^b	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 4.5 A	16	nC
Gate-Source Charge ^b	Q _{gs}		4	
Gate-Drain Charge ^b	Q _{gd}		3	
Turn-On Delay Time ^b	t _{d(on)}	V _{DD} = 30 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6Ω	10	ns
Rise Time ^b	t _r		12	
Turn-Off Delay Time ^b	t _{d(off)}		22	
Fall Time ^b	t _f		28	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2 A, di/dt = 100 A/μs	35	

Notes

- a. For design aid only; not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^{\circ}\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.