

N- and P-Channel 20-V (D-S) MOSFET

CHARACTERISTICS

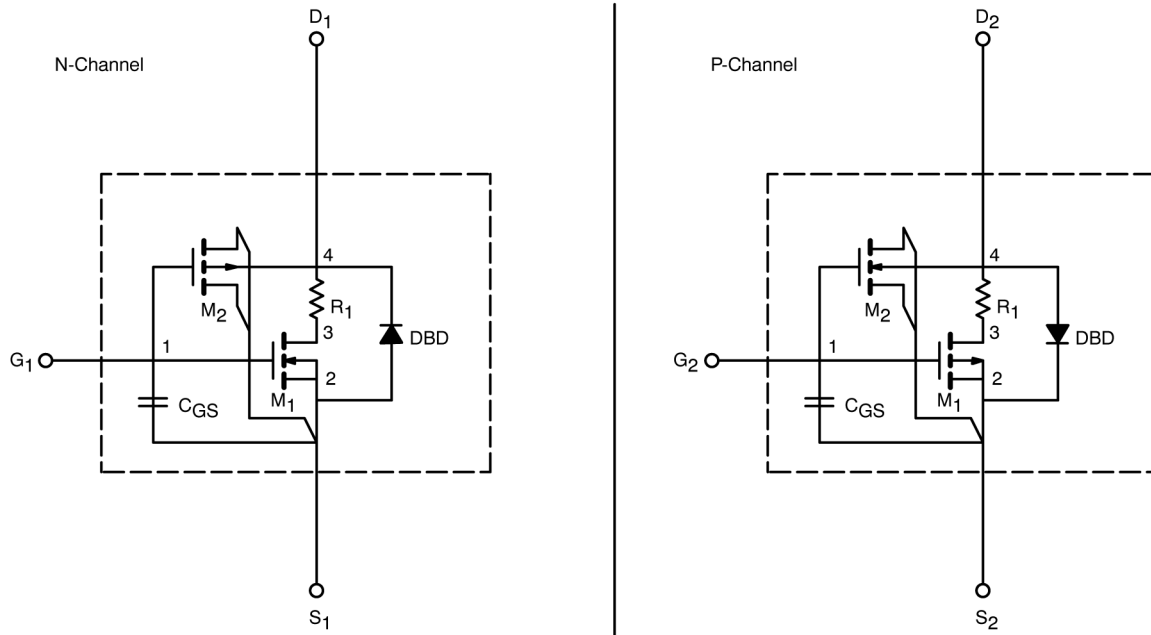
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The model subcircuit schematic is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model Si6562DQ

Vishay Siliconix



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions		Typical	Unit	
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V, V _{GS} , I _D = 250 μA	N-Ch	0.89	V	
		V _{DS} = V, V _{GS} , I _D = -250 μA	P-Ch	0.95		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	119	A	
		V _{DS} ≥ -5 V, V _{GS} = -4.5 V	P-Ch	74		
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.5 A	N-Ch	0.022	Ω	
		V _{GS} = -4.5 V, I _D = 3.5 A	P-Ch	0.040		
		V _{GS} = 2.5 V, I _D = 3.9 A	N-Ch	0.028		
		V _{GS} = -2.5 V, I _D = 2.7 A	P-Ch	0.056		
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 4.5 A	N-Ch	20	S	
		V _{DS} = -10 V, I _D = -3.5 A	P-Ch	12		
Diode Forward Voltage ^a	V _{SD}	I _S = 1.25 A, V _{GS} = 0 V	N-Ch	0.65	V	
		I _S = -1.25 A, V _{GS} = 0 V	P-Ch	-0.72		
Dynamic^b						
Total Gate Charge	Q _g	N-Channel V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 4.5 A P-Channel V _{DS} = -15 V, V _{GS} = -4.5 V, I _D = -3.5 A	N-Ch	13	nC	
			P-Ch	14.6		
Gate-Source Charge	Q _{gs}		N-Ch	3		
			P-Ch	3.5		
Gate-Drain Charge	Q _{gd}		N-Ch	3.3		
			P-Ch	3.5		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω	N-Ch	7	ns	
			P-Ch	29		
Rise Time	t _r		N-Ch	40		
			P-Ch	35		
Turn-Off Delay Time	t _{d(off)}		N-Ch	51		
			P-Ch	37		
Fall Time	t _f		N-Ch	17		
			P-Ch	50		
Source-Drain Reverse Recovery Time	t _{rr}		I _F = A, I _S = 1.25A, di/dt = 100 A/μs	N-Ch		31
			I _F = A, I _S = -1.25A, di/dt = 100 A/μs	P-Ch		59

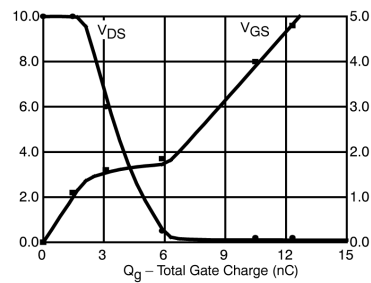
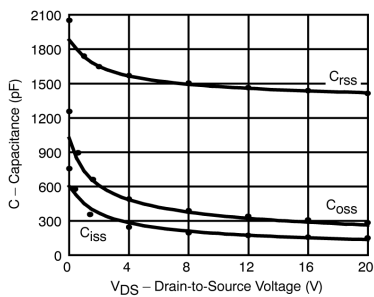
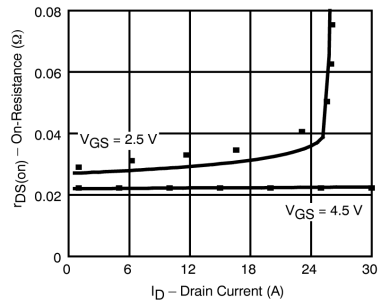
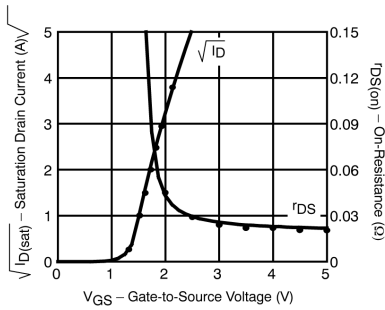
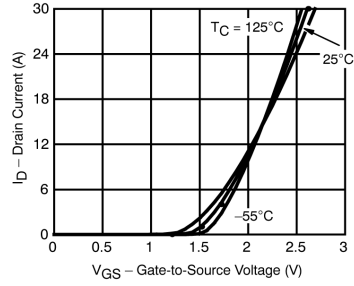
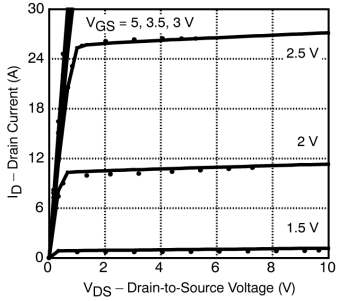
Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

N-CHANNEL MOSFET



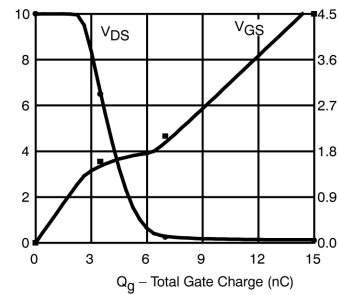
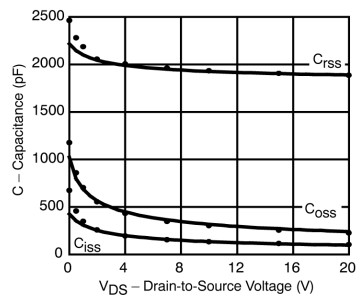
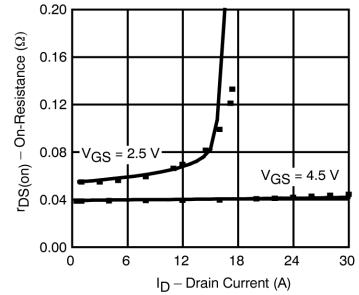
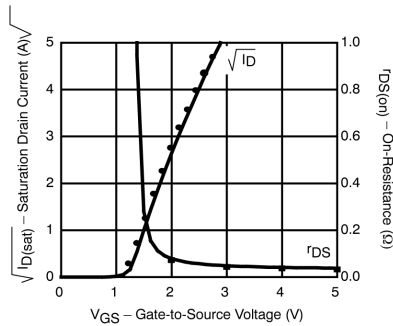
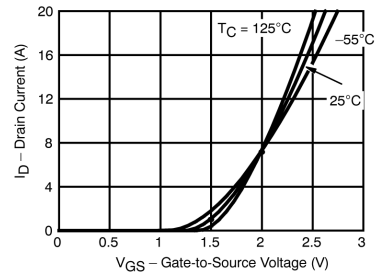
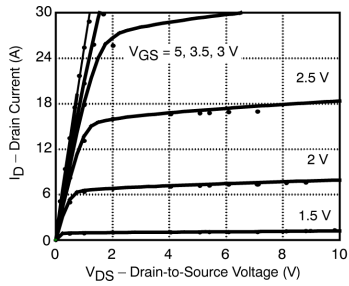
Note: Dots and squares represent measured data.

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P-CHANNEL MOSFET



Note: Dots and squares represent measured data.