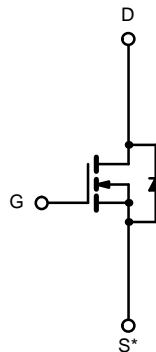
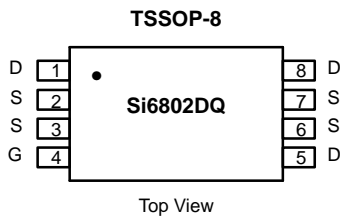




N-Channel, Reduced Q_g , Fast Switching MOSFET

High-Efficiency
PWM Optimized

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.075 @ $V_{GS} = 4.5$ V	± 3.3
	0.110 @ $V_{GS} = 3.0$ V	± 2.7



*Source Pins 2, 3, 6, and 7 must be tied common.

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 3.3	A
	$T_A = 70^\circ\text{C}$		± 2.6	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a		I_S	1.25	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.5	W
	$T_A = 70^\circ\text{C}$		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	83	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.



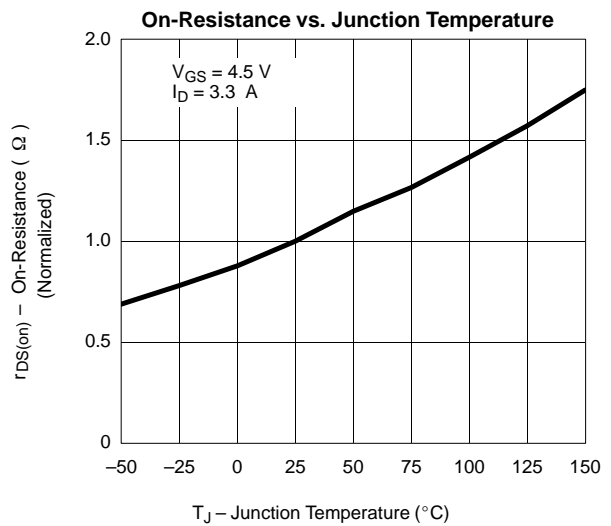
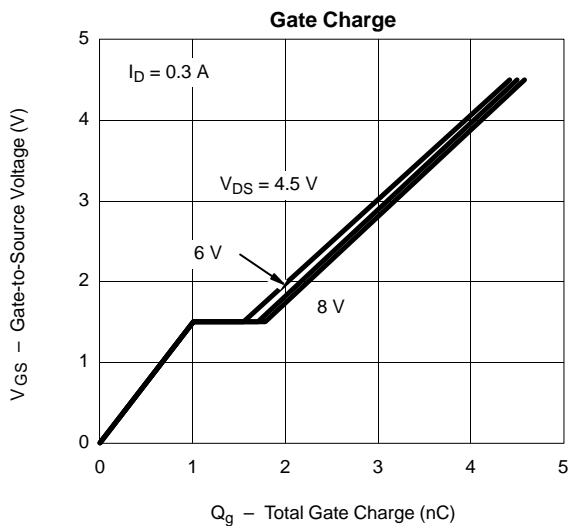
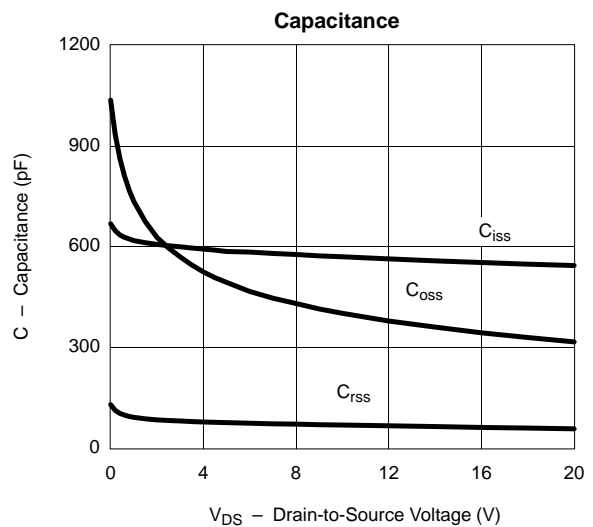
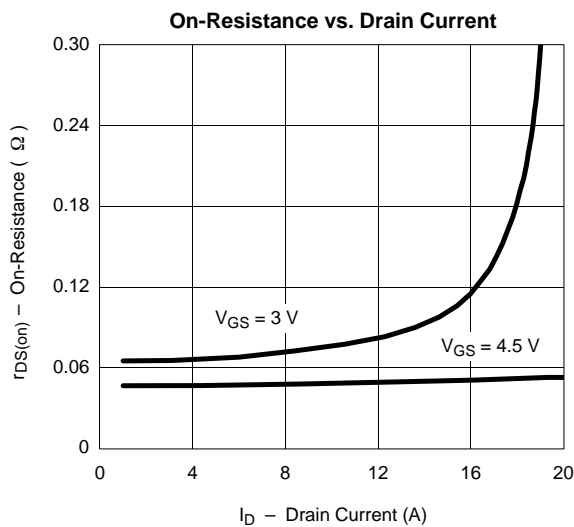
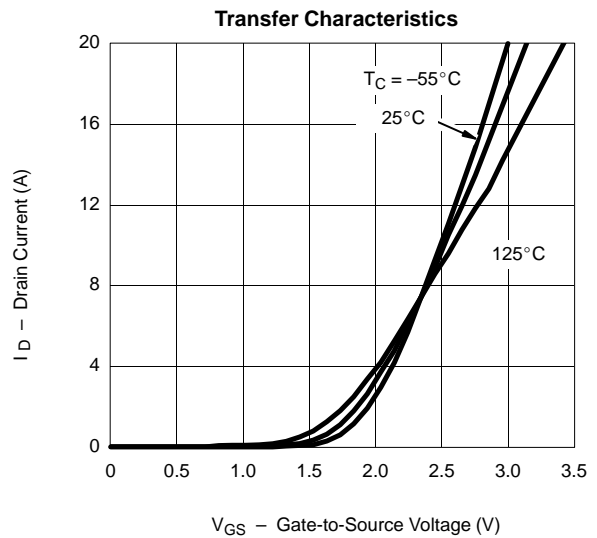
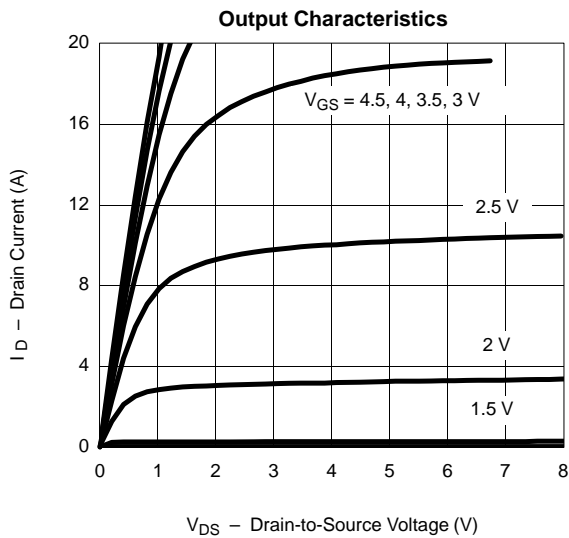
SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C			25	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	15			A
		V _{DS} ≥ 5 V, V _{GS} = 3.0 V	6			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 3.3 A		0.048	0.075	Ω
		V _{GS} = 3.0 V, I _D = 2.7 A		0.067	0.110	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 3.3 A		10.3		S
Diode Forward Voltage ^a	V _{SD}	I _S = 1.25 A, V _{GS} = 0 V		0.7	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 0.3 A		4.5	9.0	nC
Gate-Source Charge	Q _{gs}			1.0		
Gate-Drain Charge	Q _{gd}			0.7		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 6 V, R _L = 20 Ω I _D ≅ 0.3 A, V _{GEN} = 4.5 V, R _G = 6 Ω		8	20	ns
Rise Time	t _r			6	15	
Turn-Off Delay Time	t _{d(off)}			12	25	
Fall Time	t _f			16	30	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.25 A, di/dt = 100 A/μs		52	80	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

