Dual P-Channel Enhancement-Mode MOSFET

CHARACTERISTICS

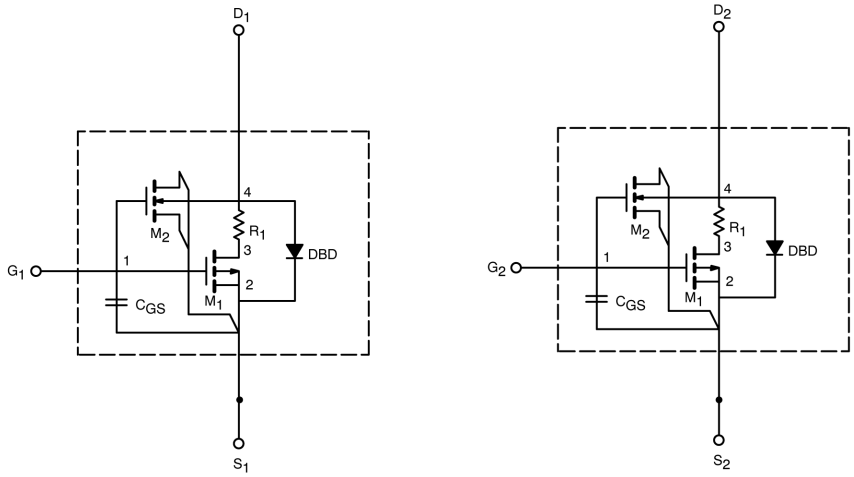
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit mode is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-to-10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

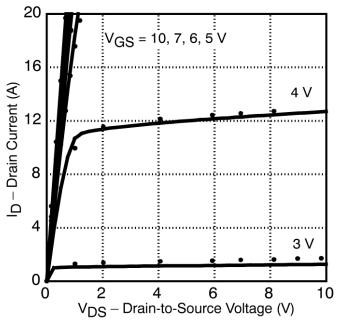


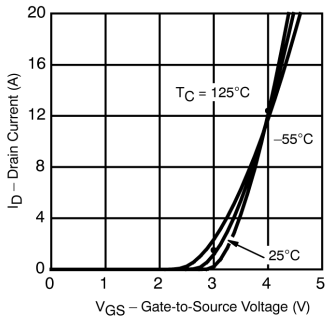
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

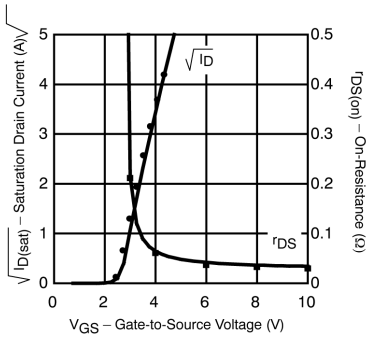
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = – 250µA	2.13		V
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} > – 5V, V_{GS} = – 10V	132		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = – 10V, I_D = – 3.5A	0.034	0.035	Ω
		V_{GS} = – 4.5V, I_D = – 2.5A	0.054	0.062	
Forward Transconductance[a]	g_{fs}	V_{DS} = – 15V, I_D = – 3.5A	9.6	7.2	S
Diode Forward Voltage[a]	V_{SD}	I_S = – 1.25A, V_{GS} = 0V	- 0.78	- 0.77	V
Dynamic[b]					
Total Gate Charge	Q_g	V_{DS} = – 15V, V_{GS} = – 10V, I_D = – 3.5A	18	17	nC
Gate-Source Charge	Q_{gs}		4.4	4.4	
Gate-Drain Charge	Q_{gd}		3.1	3.1	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = – 15V, R_L = 15Ω I_D ≅ – 1A, V_{GEN} = – 10V, R_G = 6Ω	14	13	ns
Rise Time	t_r		7.8	10	
Turn-Off Delay Time	$t_{d(off)}$		21	33	
Fall Time	t_f		11	10	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = – 1.25A, di/dt = 100A/µs	30	30	

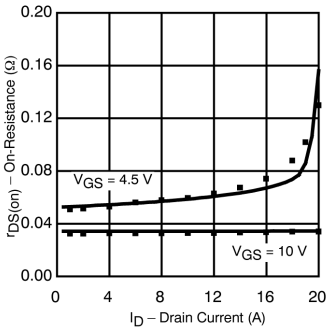
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

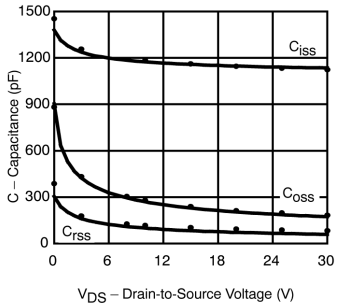
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

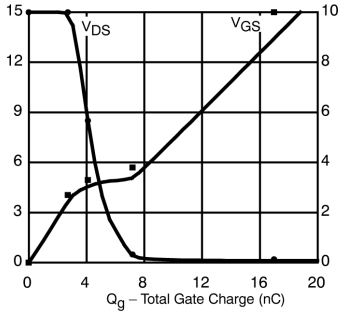












Note: Dots and squares represent measured data.