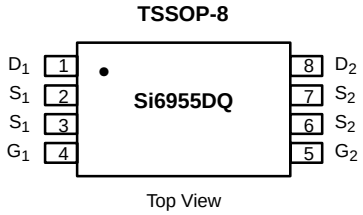
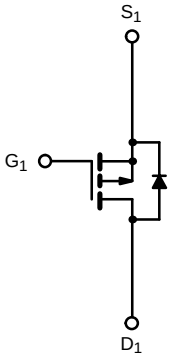
Dual P-Channel 30-V (D-S) MOSFET

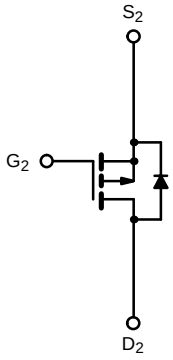
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(ON)}$ (Ω)	I_D (A)
–30	0.085 @ V_{GS} = –10 V	± 2.5
	0.19 @ V_{GS} = –4.5 V	± 1.8



Top View



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[A]	T_A = 25°C	I_D	± 2.5	A
	T_A = 70°C		± 2.1	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[A]		I_S	–1.25	
Maximum Power Dissipation[A]	T_A = 25°C	P_D	1.0	W
	T_A = 70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Maximum Junction-to-Ambient[A]	R_{thJA}	125	°C/W

Notes
A. Surface Mounted on FR4 Board, t ≤ 10 sec.

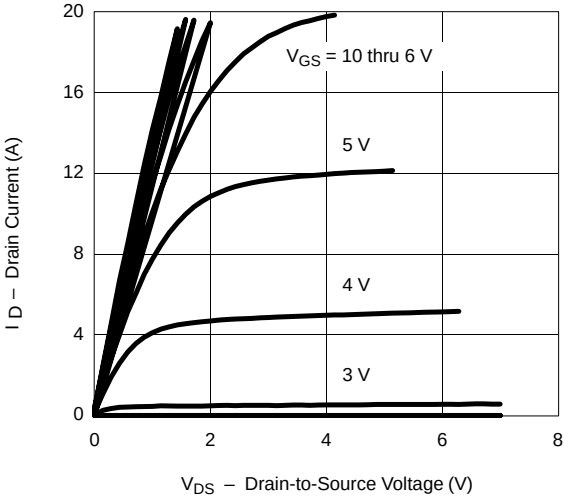
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70180.
For SPICE model information via the Worldwide Web: http://www.siliconix.com/www/product/spice.htm

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
PARAMETER	**SYMBOL**	**TEST CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
STATIC						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250 μA	–1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1	μA
		V_{DS} = –30 V, V_{GS} = 0 V, T_J = 55°C			–25	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} ≥ –5 V, V_{GS} = –10 V	–15			A
Drain-Source On-State Resistance[A]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = –2.5 A		0.066	0.085	Ω
		V_{GS} = –4.5 V, I_D = –1.8 A		0.125	0.19	
Forward Transconductance[A]	g_{fs}	V_{DS} = –15 V, I_D = –2.5 A		5		S
Diode Forward Voltage[A]	V_{SD}	I_S = –1.25 A, V_{GS} = 0 V		0.8	–1.2	V
DYNAMIC[B]						
Total Gate Charge	Q_g	V_{DS} = –10 V, V_{GS} = –10 V, I_D = –2.5 A		8.7	15	nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –10 V, R_L = 10 Ω I_D ≅ –1 A, V_{GEN} = –10 V, R_G = 6 Ω		7	15	ns
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			14	27	
Fall Time	t_f			8	15	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –1.25 A, di/dt = 100 A/μs		46	80	

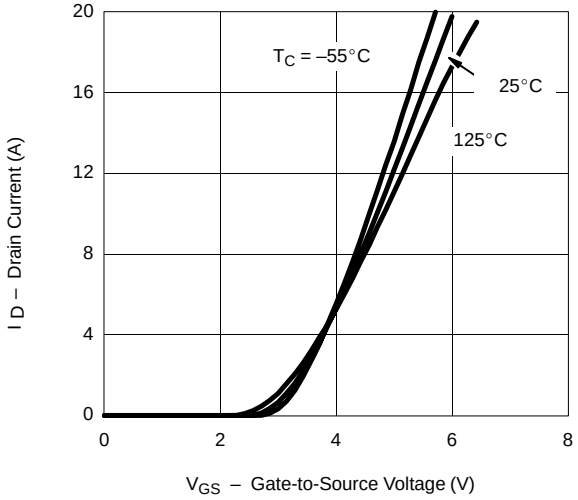
Notes
A. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
B. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

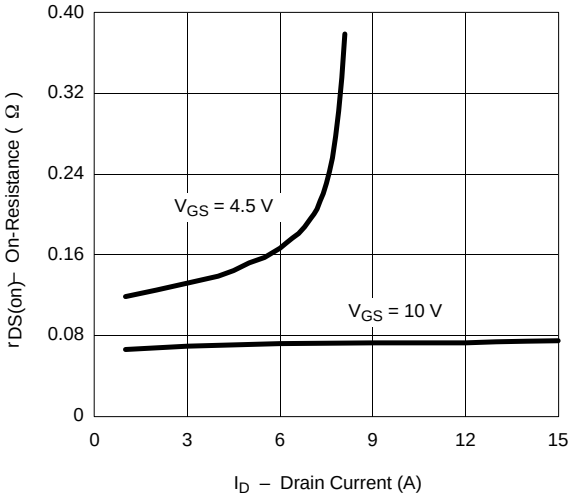
Output Characteristics



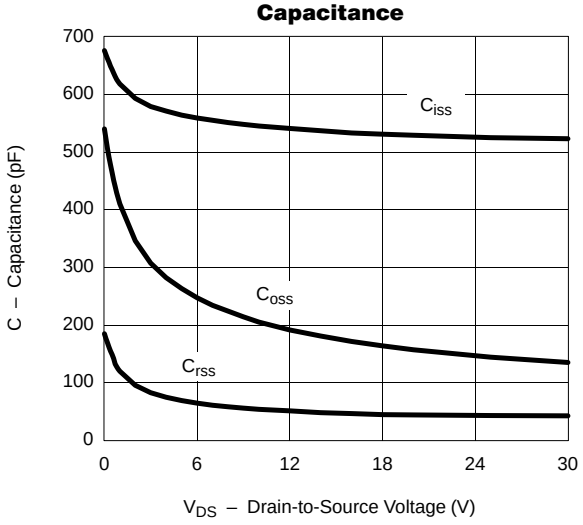
Transfer Characteristics



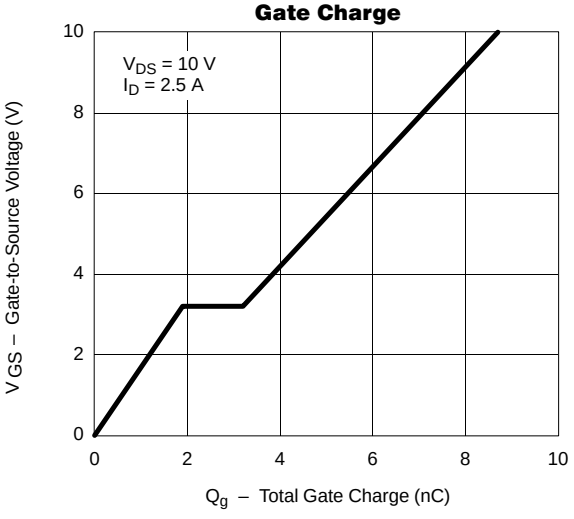
On-Resistance vs. Drain Current



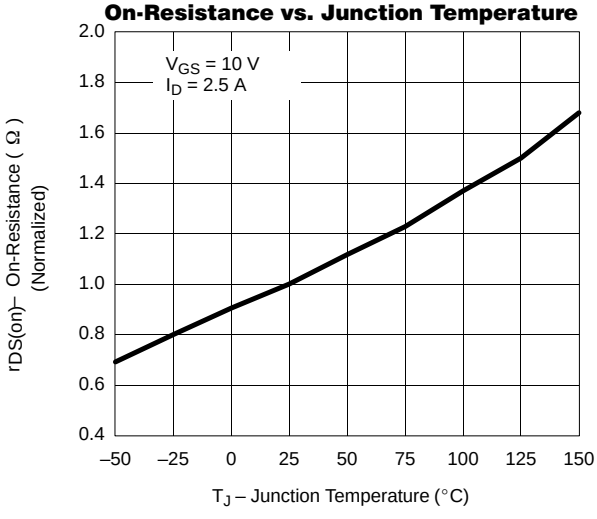
Capacitance



Gate Charge

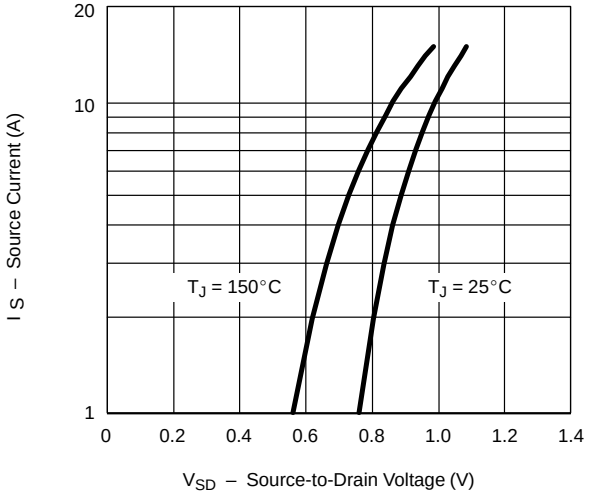


On-Resistance vs. Junction Temperature

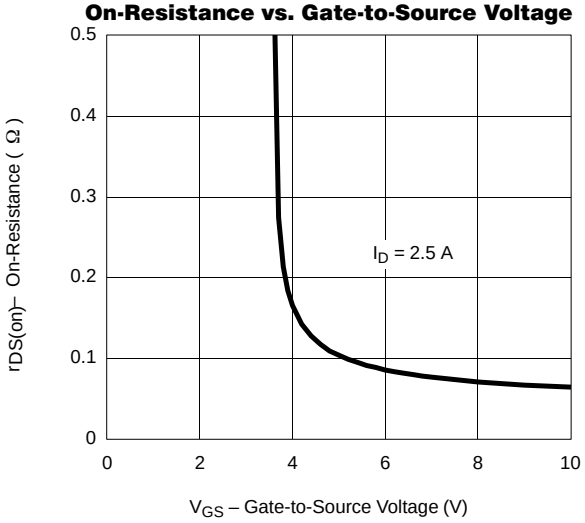


TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

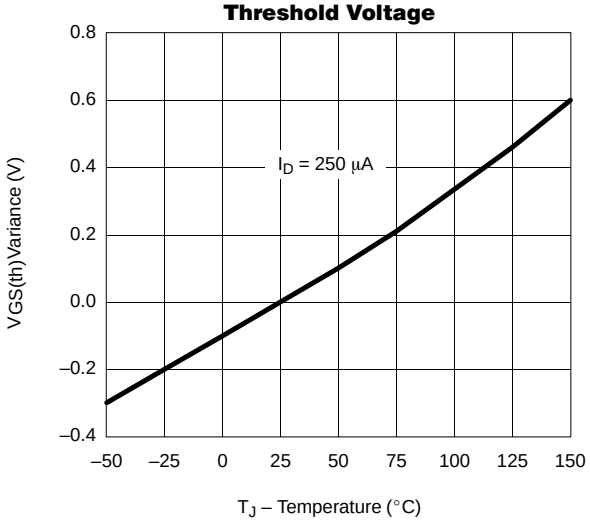
Source-Drain Diode Forward Voltage



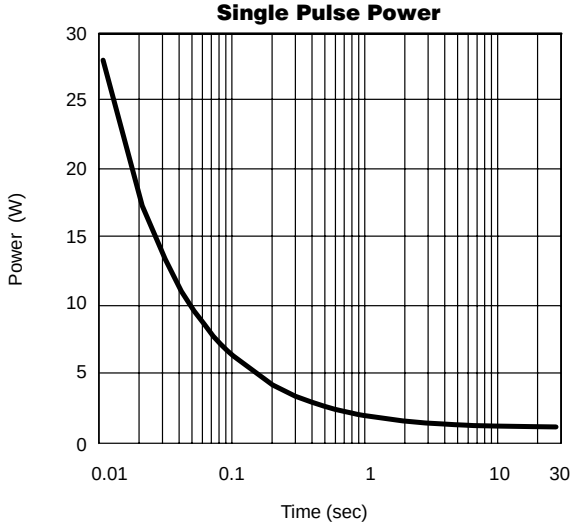
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient