

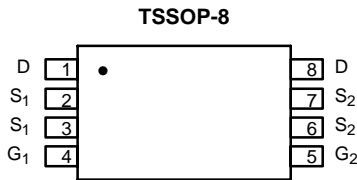
Dual N-Channel 2.5-V (G-S) MOSFET Common Drain, ESD Protection

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.022 @ $V_{GS} = 4.5$ V	6.5
	0.030 @ $V_{GS} = 2.5$ V	5.5

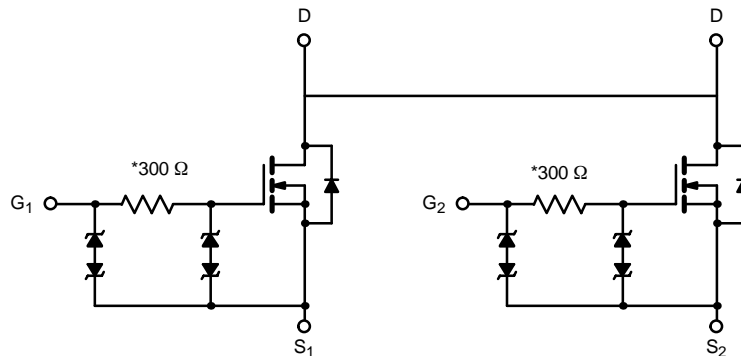
FEATURES

- TrenchFET® Power MOSFET
- ESD Protected: 3000 V



Top View

Ordering Information:
Si6968BEDQ-T1 (with Tape and Reel)



*Typical value by design

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	20		V	
Gate-Source Voltage	V_{GS}	± 12			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	6.5	5.2	A
		$T_A = 70^\circ\text{C}$	5.5	3.5	
Pulsed Drain Current	I_{DM}	30			
Continuous Source Current (Diode Conduction) ^a	I_S	1.5	1.0	W	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	1.5		1.0
		$T_A = 70^\circ\text{C}$	0.96		0.64
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typ	Max	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	72	83	$^\circ\text{C/W}$
		Steady-State	100	120	
Maximum Junction-to-Foot (Drain)	R_{thJF}	55	70		

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

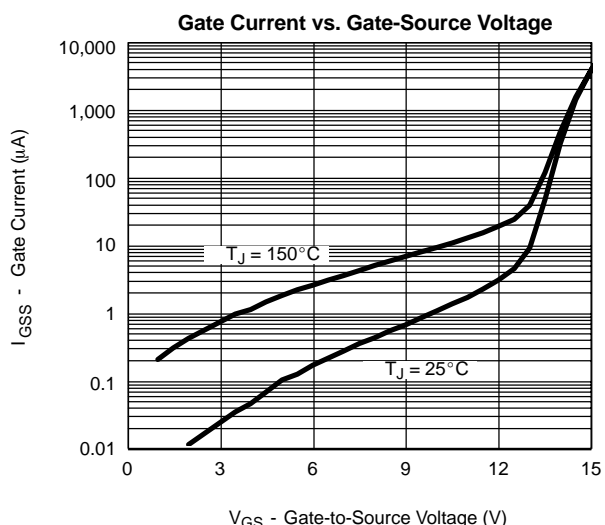
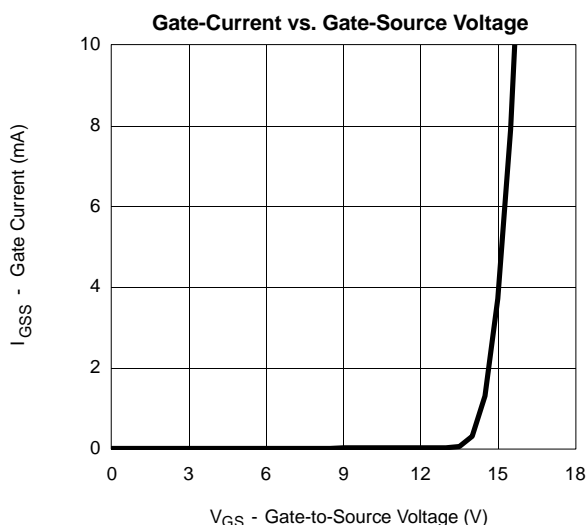


SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6		1.6	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±4.5 V			±200	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V			1	μA
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 70 °C			25	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≤ 5 V, V _{GS} = 4.5 V	30			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 6.5 A		0.0165	0.022	Ω
		V _{GS} = 2.5 V, I _D = 5.5 A		0.023	0.030	
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 6.5 A		30		S
Diode Forward Voltage ^b	V _{SD}	I _S = 1.5 A, V _{GS} = 0 V		0.71	1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 6.5 A		12	18	nC
Gate-Source Charge	Q _{gs}			2.2		
Gate-Drain Charge	Q _{gd}			3.6		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω		245	365	ns
Rise Time	t _r			330	495	
Turn-Off Delay Time	t _{d(off)}			860	1300	
Fall Time	t _f			510	765	

Notes

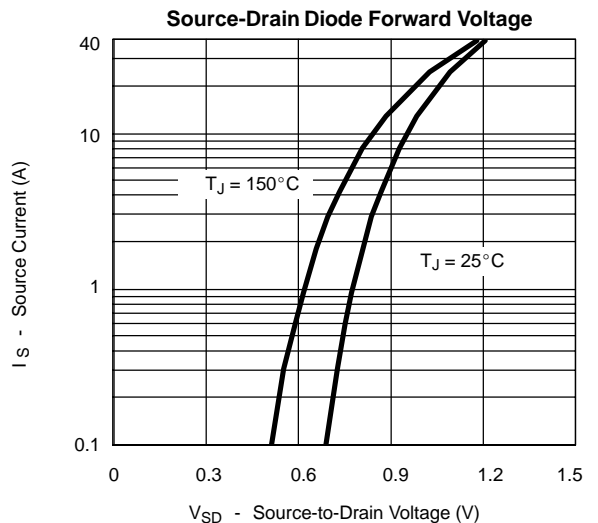
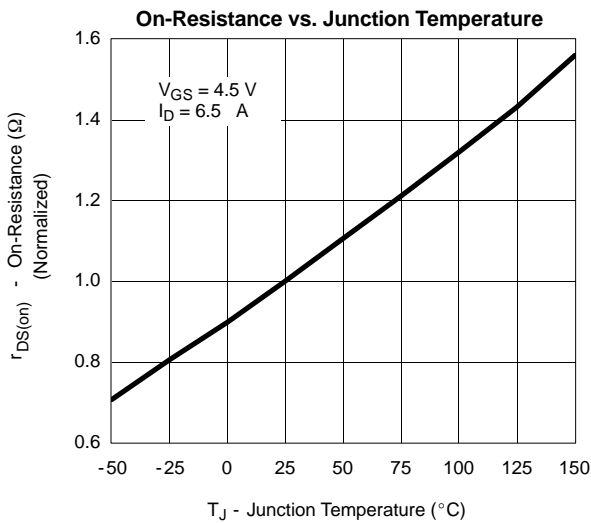
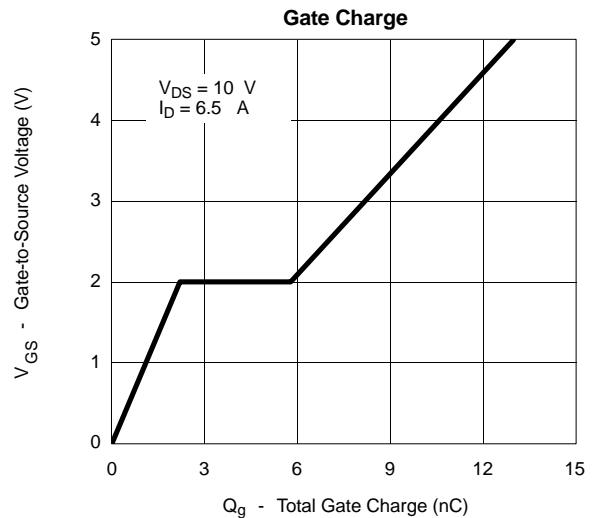
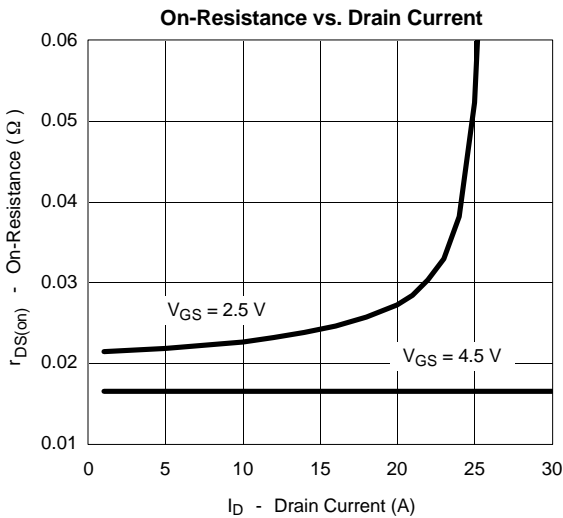
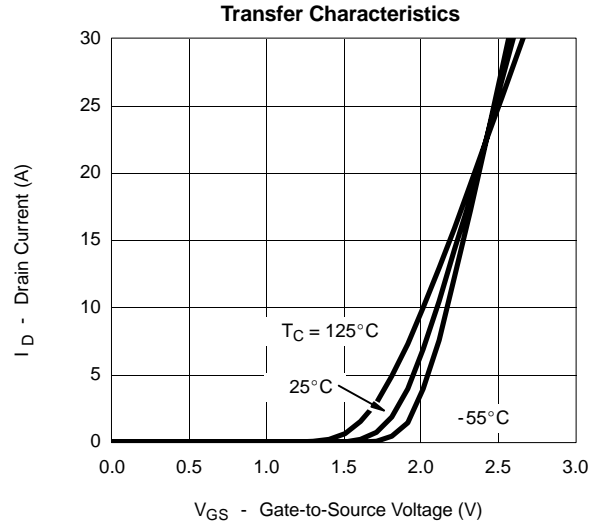
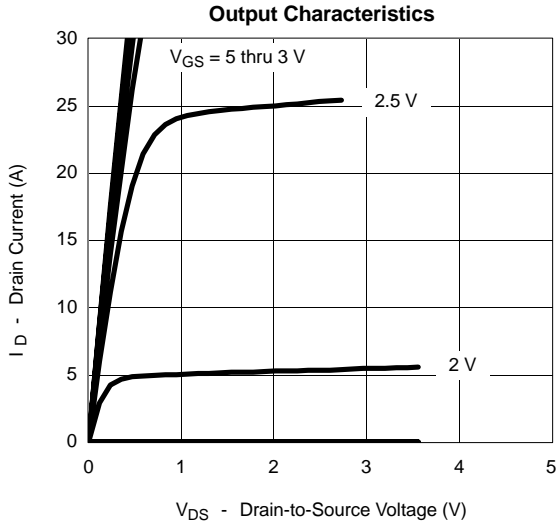
- a. For design aid only; not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

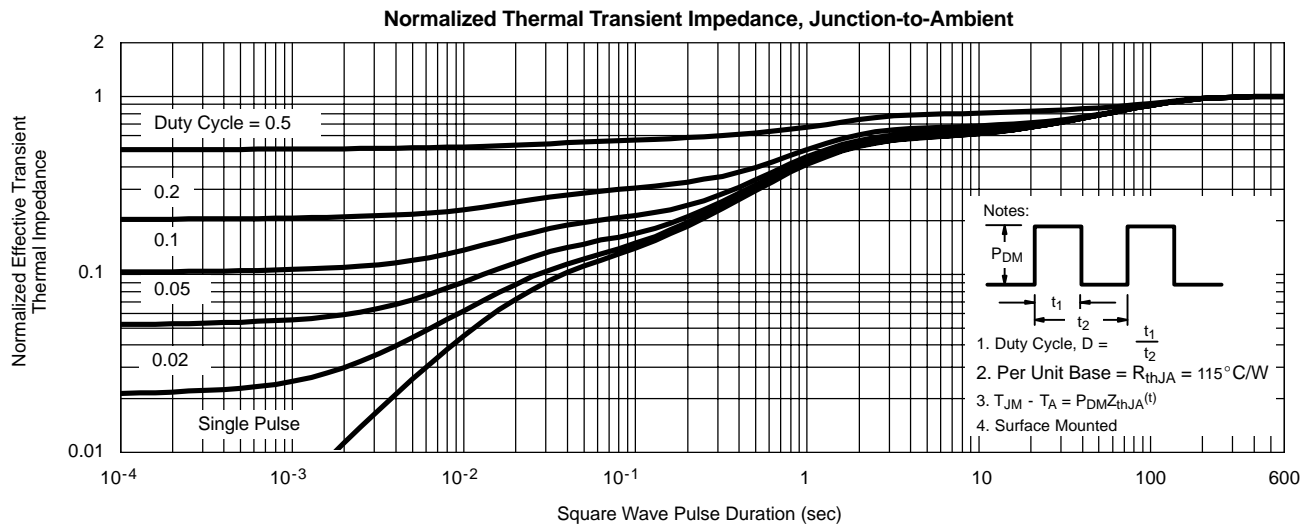
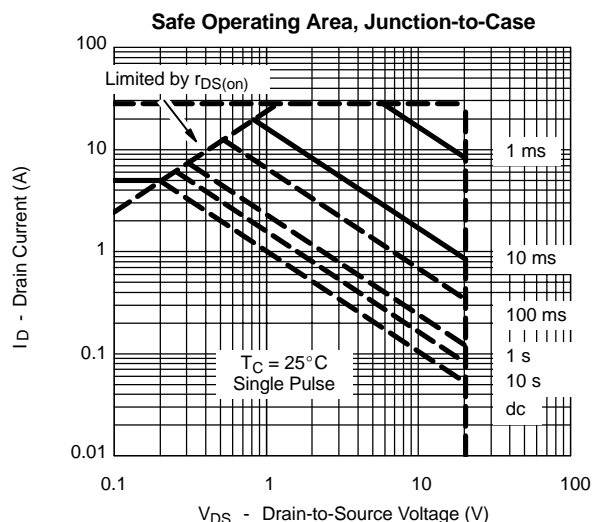
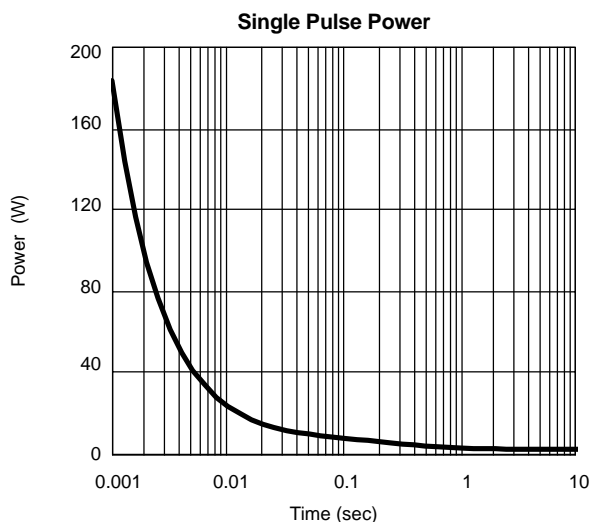
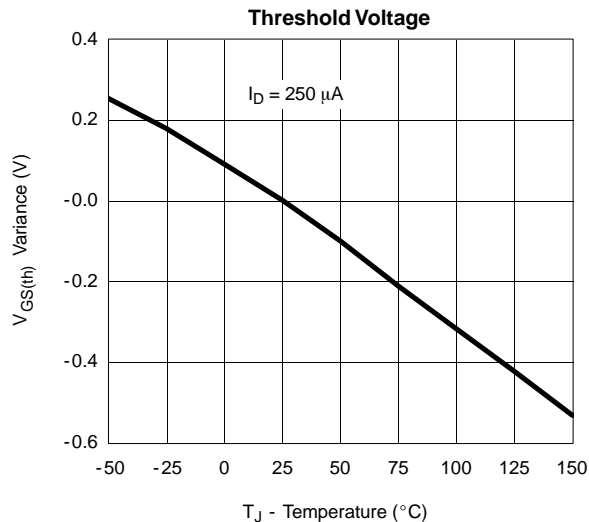
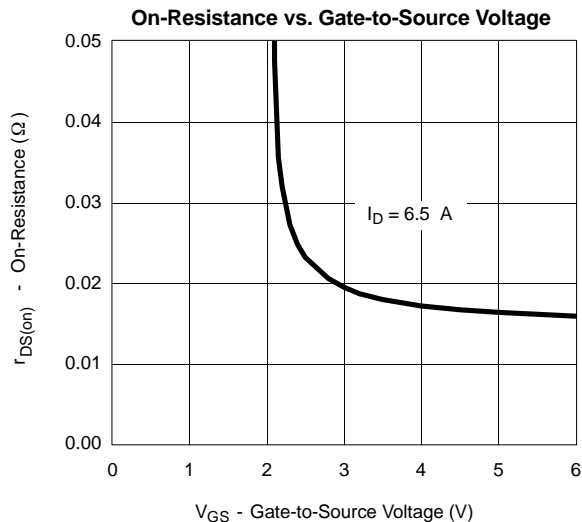




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