



N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.0125 @ $V_{GS} = 10$ V	14
	0.020 @ $V_{GS} = 4.5$ V	11

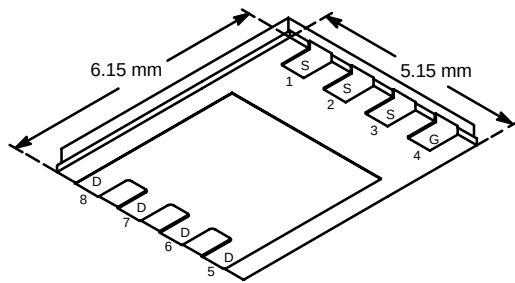
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile
- PWM Optimized

APPLICATIONS

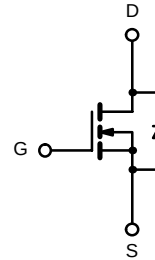
- DC/DC conversion High-Side
 - Desktop
 - Server
- Synchronous Rectification

PowerPAK™ SO-8



Bottom View

Ordering Information: Si7348DP-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	20		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	14	9.0	A
	T _A = 70°C		11	7.0	
Pulsed Drain Current (10 μs Pulse Width)		I _{DM}	50		
Continuous Source Current (Diode Conduction) ^a		I _S	3.7	1.6	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	4.1	1.8	W
	T _A = 70°C		2.6	1.1	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	22	30	$^\circ\text{C/W}$
	Steady State		55	70	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	6.4	8.0	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

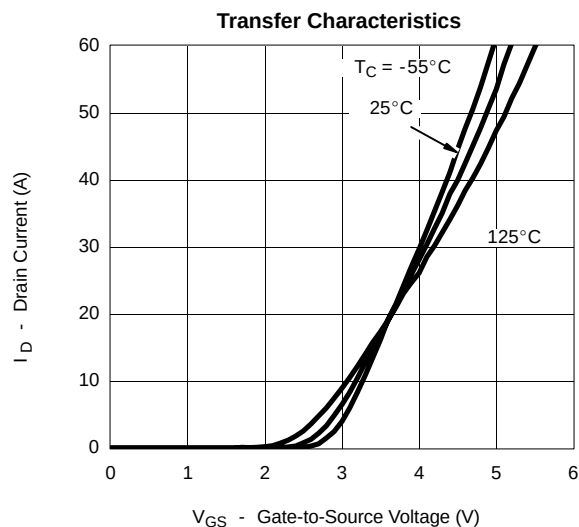
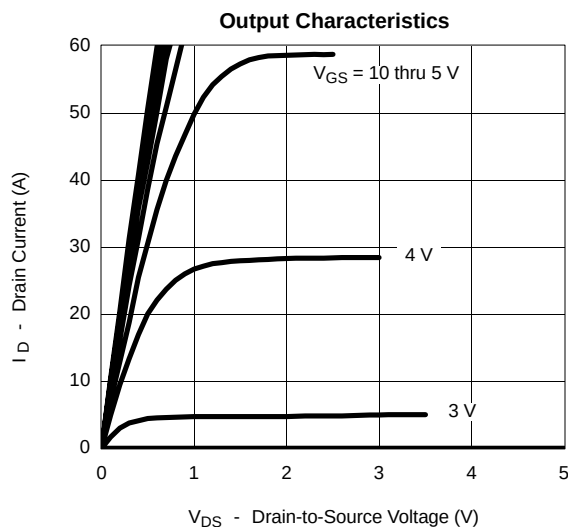
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

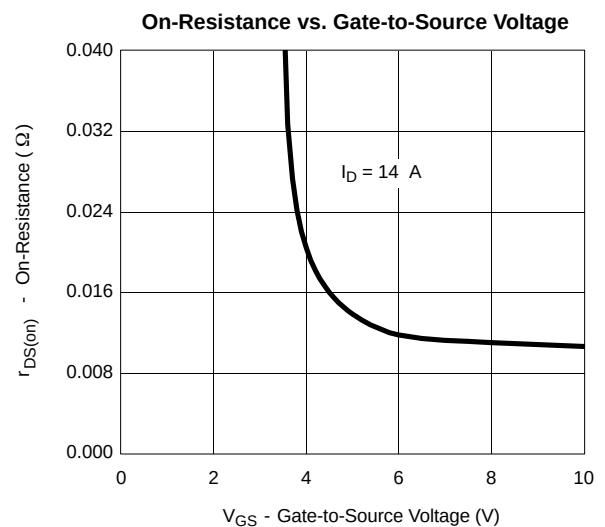
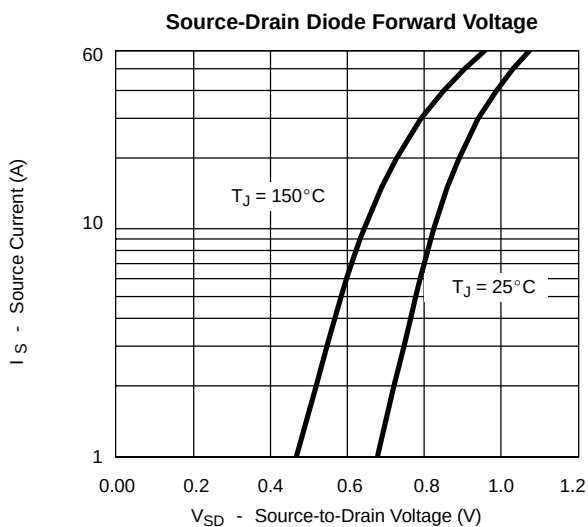
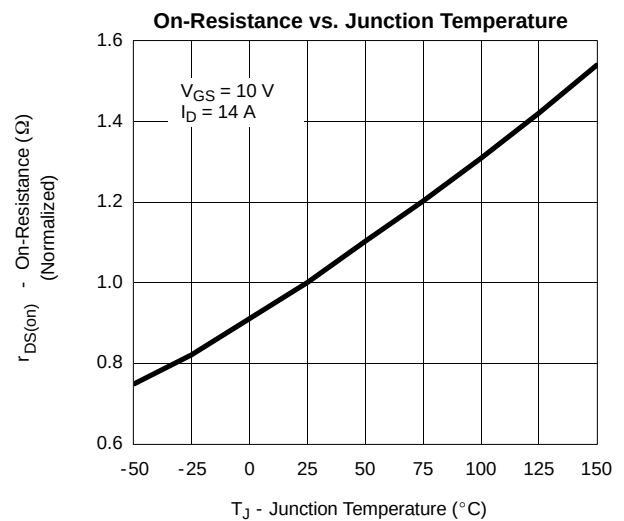
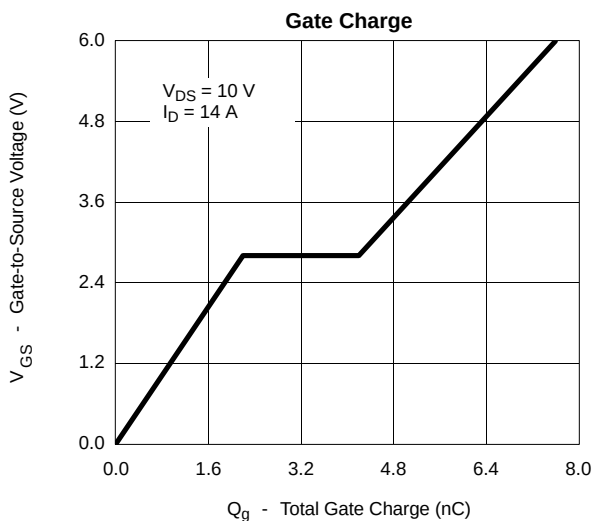
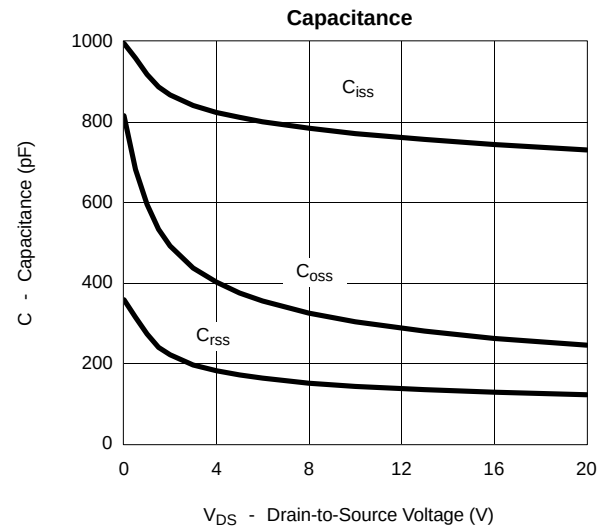
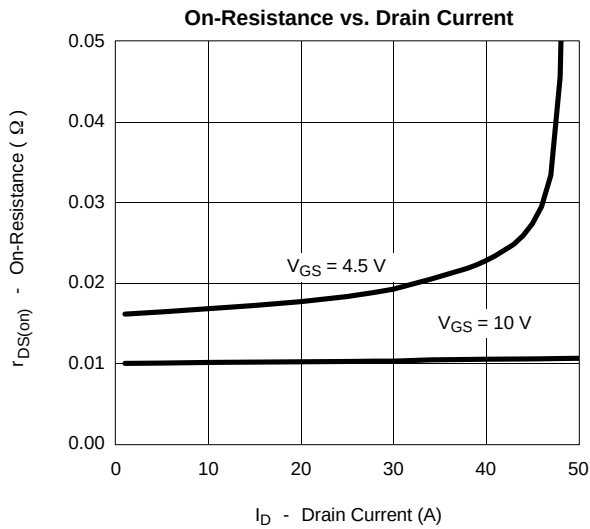
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 16\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 14\ \text{A}$		0.010	0.0125	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 11\ \text{A}$		0.016	0.020	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 6\ \text{V}$, $I_D = 14\ \text{A}$		19		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.7\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 14\ \text{A}$		5.7	8.5	nC
Gate-Source Charge	Q_{gs}			2.2		
Gate-Drain Charge	Q_{gd}			2.0		
Gate Resistance	R_g			1.3		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		17	30	ns
Rise Time	t_r			17	30	
Turn-Off Delay Time	$t_{d(off)}$			37	60	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		30	60	

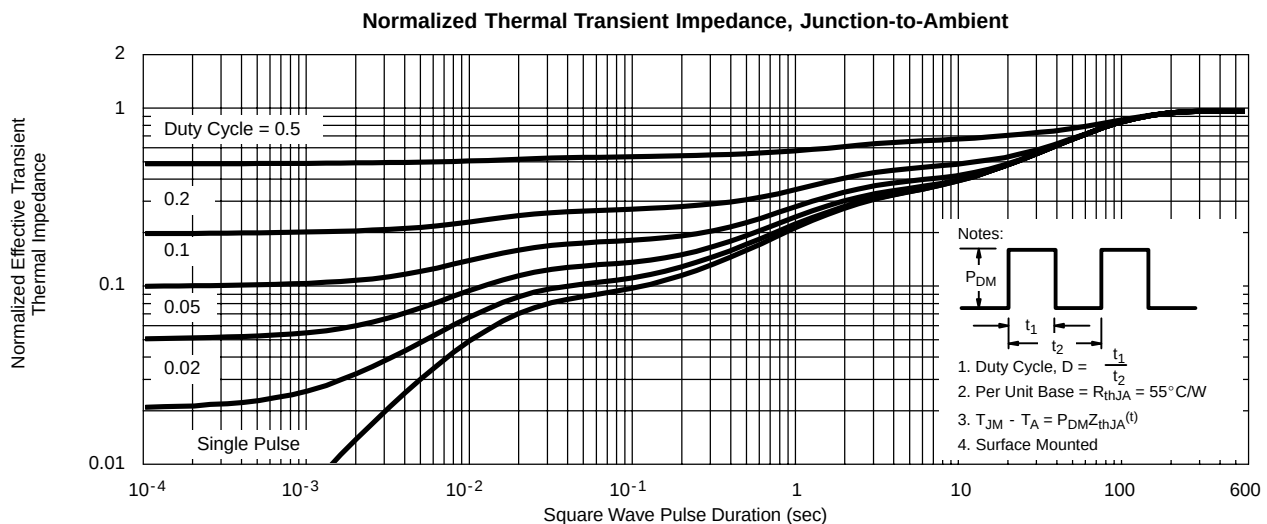
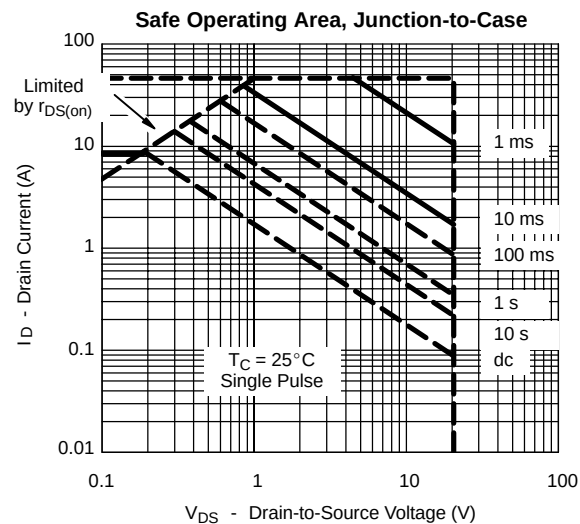
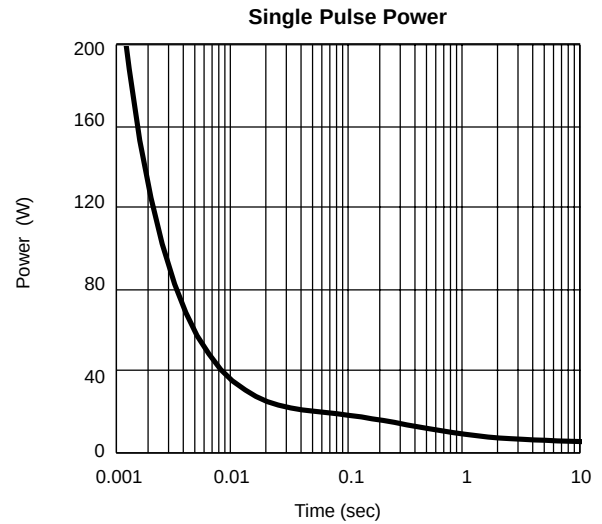
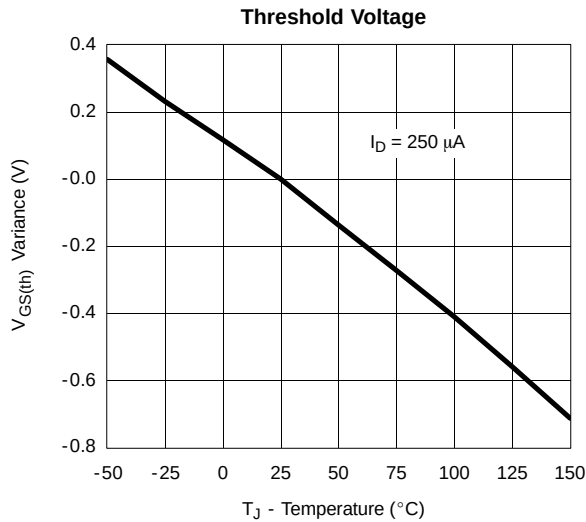
Notes

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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