N-Channel 30-V (D-S) Fast Switching WFET™

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0095 @ V_{GS} = 10 V	15
	0.0135 @ V_{GS} = 4.5 V	13

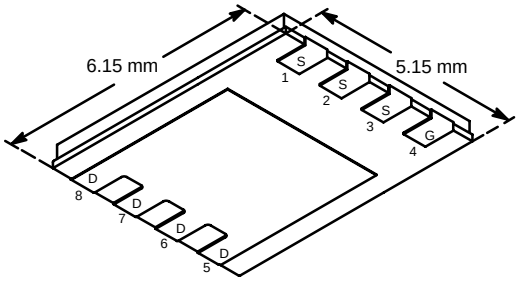
FEATURES

- Extremely Low Q_{gd} WFET Technology for Low Switching Losses
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100% R_g Tested

APPLICATIONS

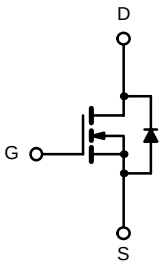
- High-Side DC/DC Conversion
  - Notebook
  - Server
  - Workstation
- Point-of-Load Conversion

PowerPAK SO-8



Bottom View

Ordering Information: Si7390DP-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	15	9	A
	T_A = 70°C		12	7	
Pulsed Drain Current		I_{DM}	±50		
Continuous Source Current (Diode Conduction)[a]		I_S	4.1	1.5	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	5	1.8	W
	T_A = 70°C		3.2	1.1	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET)[a]	t ≤ 10 sec	R_{thJA}	20	25	°C/W
	Steady State		53	70	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.1	3.2	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

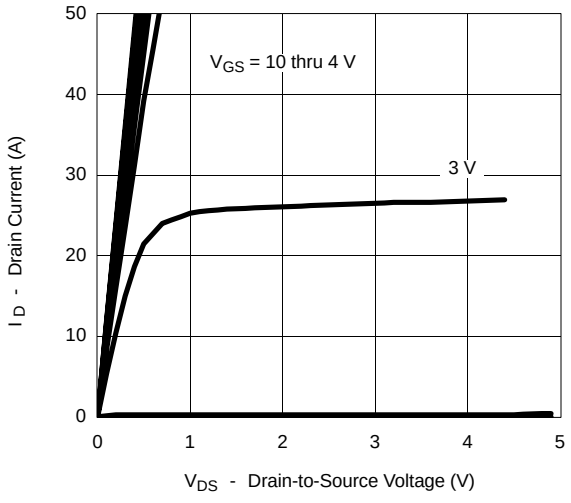
MOSFET SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	0.8		3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 70°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 15		0.0075	0.0095	Ω
		V_{GS} = 4.5 V, I_D = 13		0.0105	0.0135	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 15		45		S
Diode Forward Voltage[a]	V_{SD}	I_S = 4.1 A, V_{GS} = 0 V		0.7	1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 15 A		10	15	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			2.1		
Gate-Resistance	R_g		0.2	0.8	1.4	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		16	30	ns
Rise Time	t_r			7	12	
Turn-Off Delay Time	$t_{d(off)}$			43	70	
Fall Time	t_f			14	25	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.7 A, di/dt = 100 A/μs		35	60	

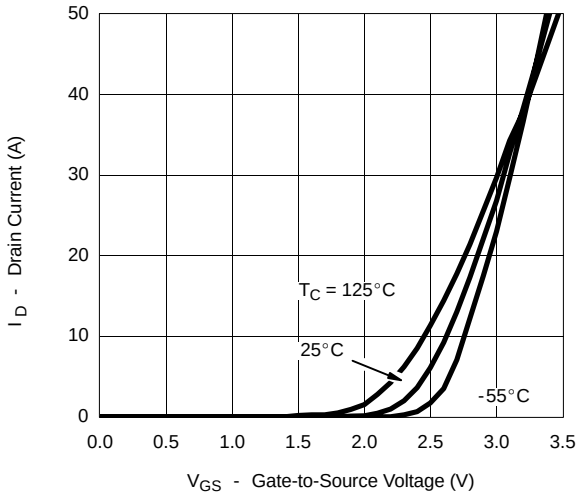
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

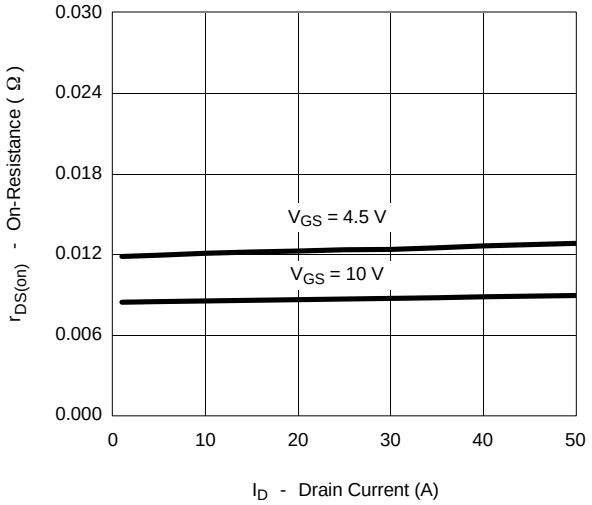


Transfer Characteristics

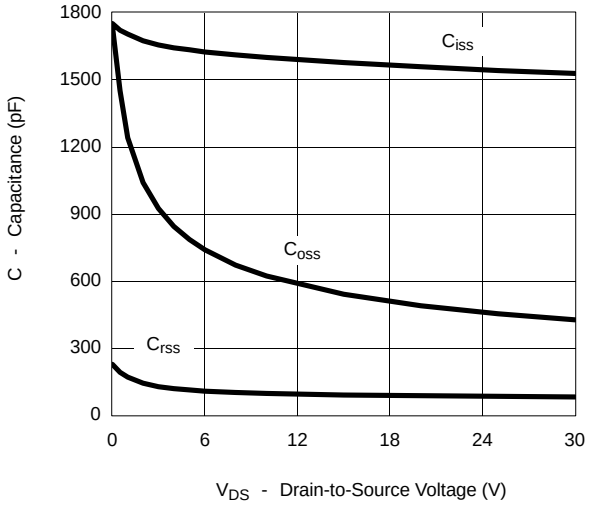


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

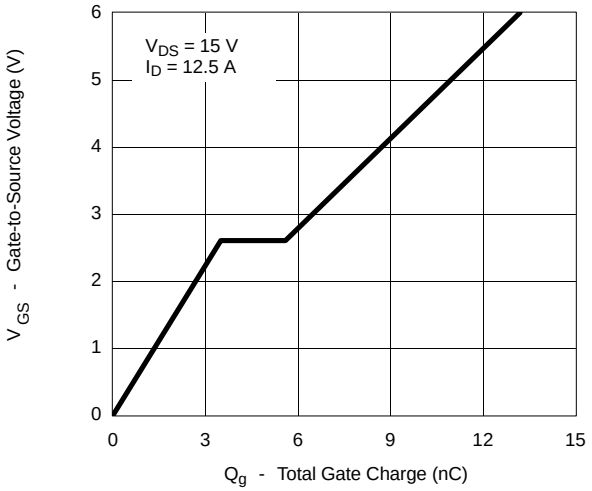
On-Resistance vs. Drain Current



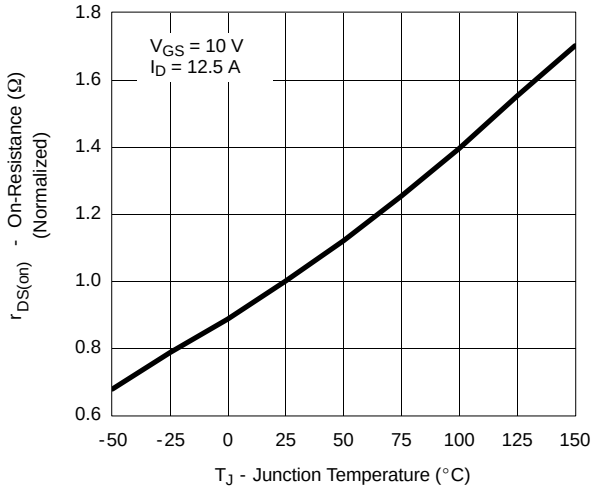
Capacitance



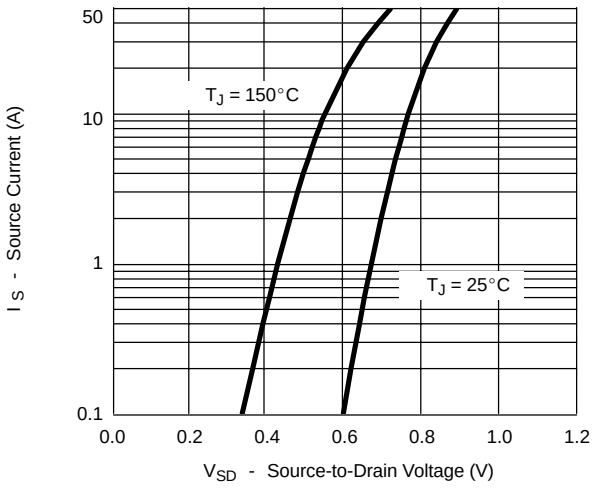
Gate Charge



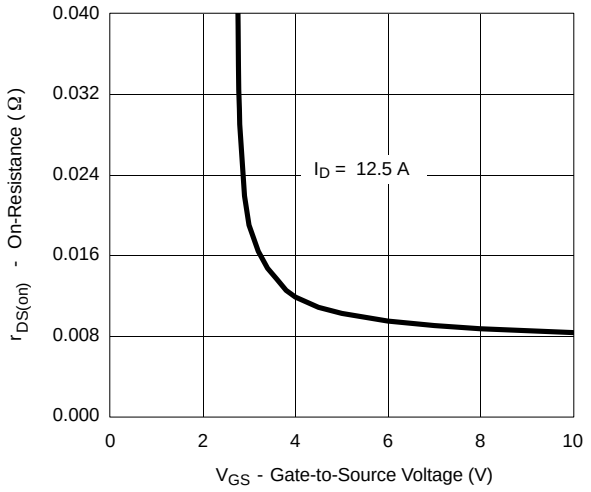
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



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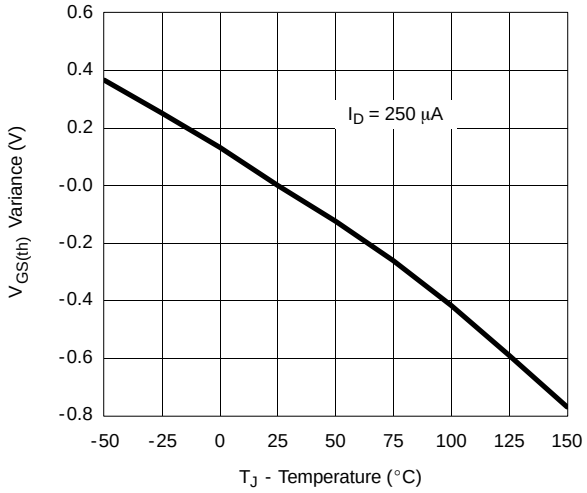
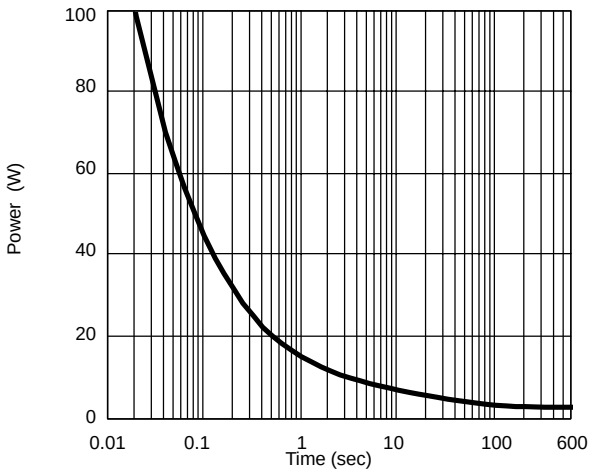
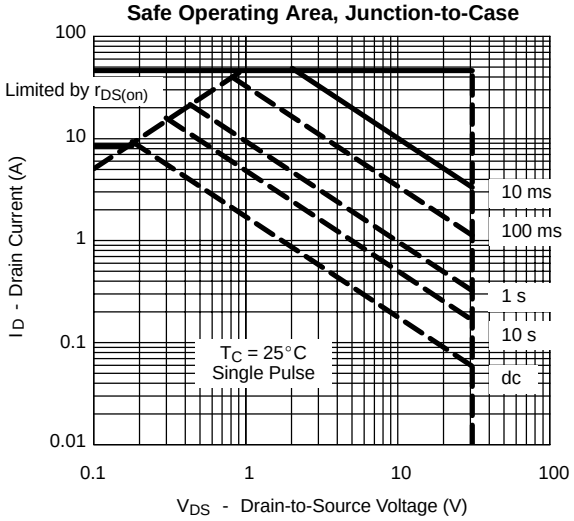
Threshold Voltage



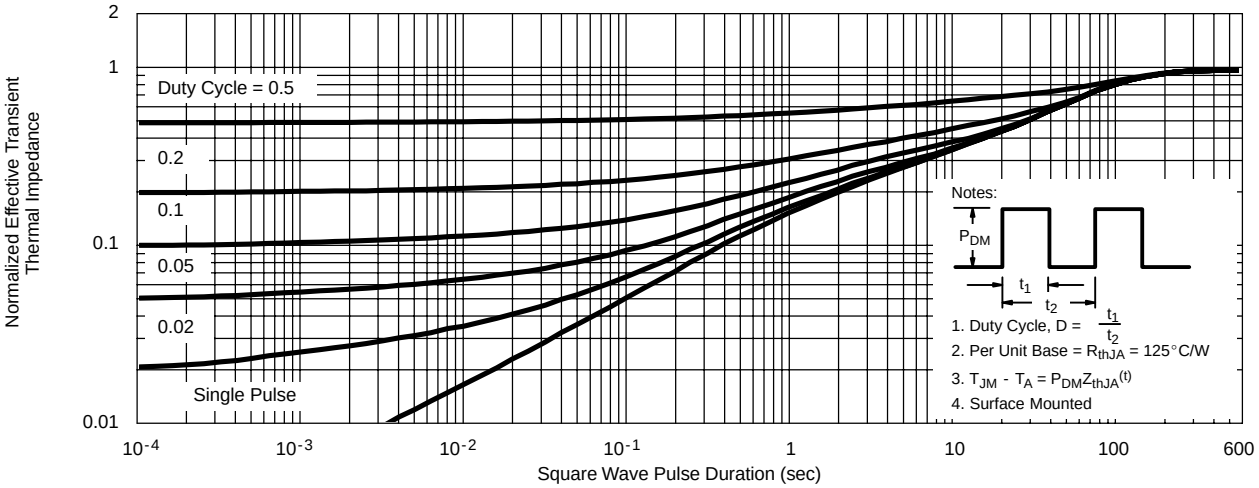
Single Pulse Power



Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)