



## N-Channel 30-V (D-S) Fast Switching MOSFET

### CHARACTERISTICS

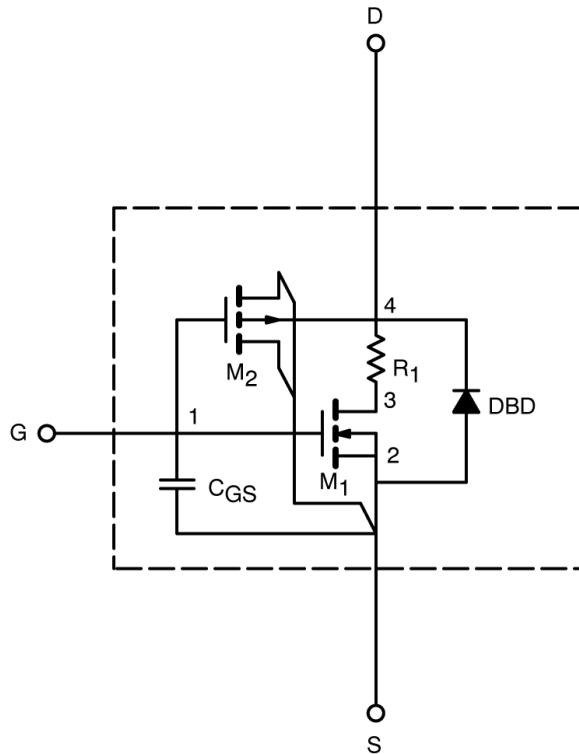
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the  $-55$  to  $125^{\circ}\text{C}$  Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the  $-55$  to  $125^{\circ}\text{C}$  temperature ranges under the pulsed 0-to-10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SPICE Device Model Si7840DP

Vishay Siliconix



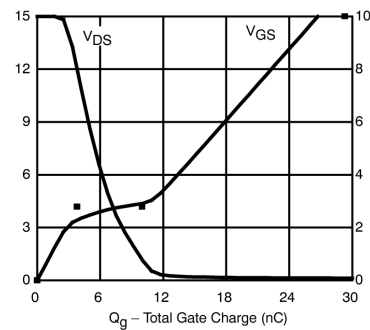
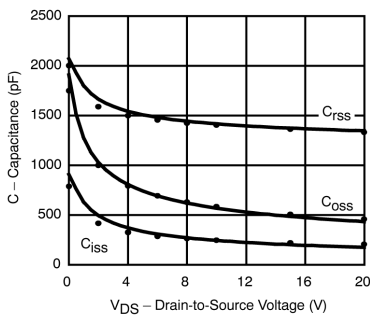
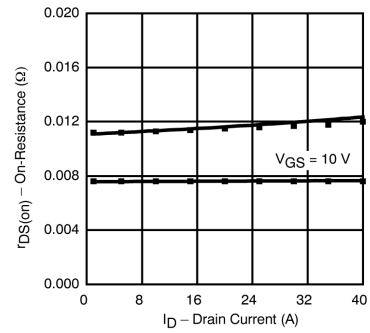
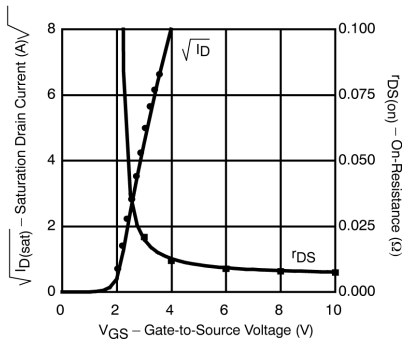
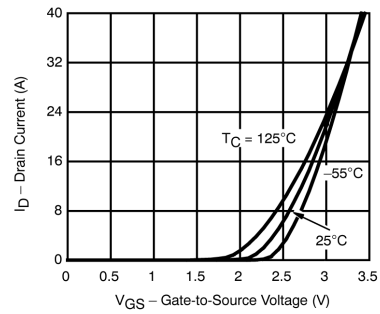
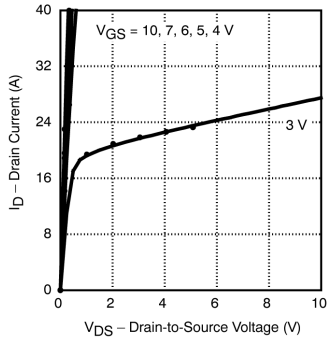
SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
<b>Static</b>					
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.2		V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5V, V <sub>GS</sub> = 10V	529		A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 18A	0.0076	0.0077	Ω
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 15A	0.0115	0.0115	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> = 18A	43	40	S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 4.1A, V <sub>GS</sub> = 0V	0.75	0.75	V
<b>Dynamic<sup>b</sup></b>					
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 5V, I <sub>D</sub> = 18A	15.4	15.5	nC
Gate-Source Charge	Q <sub>gs</sub>		3.8	3.8	
Gate-Drain Charge	Q <sub>gd</sub>		6	6	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15V, R <sub>L</sub> = 15Ω I <sub>D</sub> ≡ 1A, V <sub>GEN</sub> = 10V, R <sub>G</sub> = 6Ω	14	17	Ns
Rise Time	t <sub>r</sub>		19	14	
Turn-Off Delay Time	t <sub>d(off)</sub>		36	39	
Fall Time	t <sub>f</sub>		62	19	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 4.1A, di/dt = 100 A/μs	45	50	

**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.