



N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

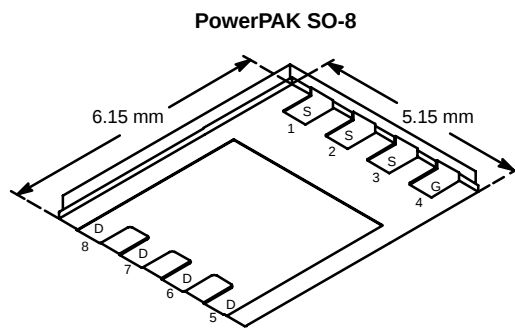
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.012 @ $V_{GS} = 10$ V	15.7
	0.020 @ $V_{GS} = 4.5$ V	12.1

FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- Optimized for “High-Side” Synchronous Rectifier Operation
- 100% R_g Tested

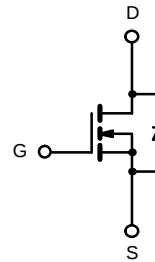
APPLICATIONS

- DC/DC Converters



Bottom View

Ordering Information: Si7888DP-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	15.7	9.4	A
	T _A = 70°C		12.5	7.5	
Pulsed Drain Current		I _{DM}	± 50		
Continuous Source Current (Diode Conduction) ^a		I _S	4.1	1.5	
Avalanche Current	L= 0.1 mH	I _{AS}	20		A
Single Pulse Avalanche Energy		E _{AS}	20		mJ
Maximum Power Dissipation ^a	T _A = 25°C	P _D	5.0	1.8	W
	T _A = 70°C		3.2	1.1	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^a	$t \leq 10$ sec	R_{thJA}	21	25	$^\circ\text{C/W}$
	Steady State		55	70	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.4	3.0	

Notes

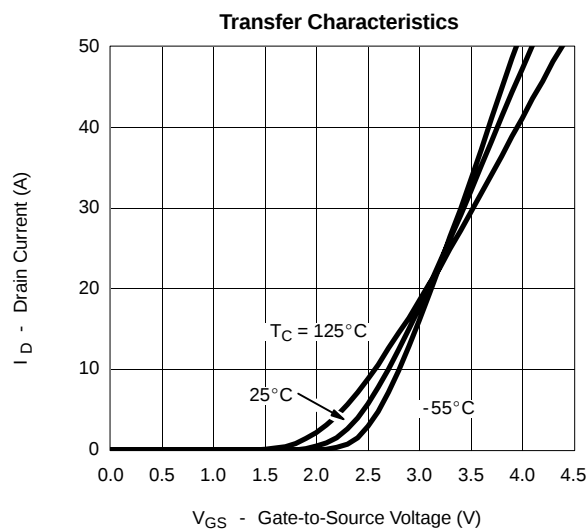
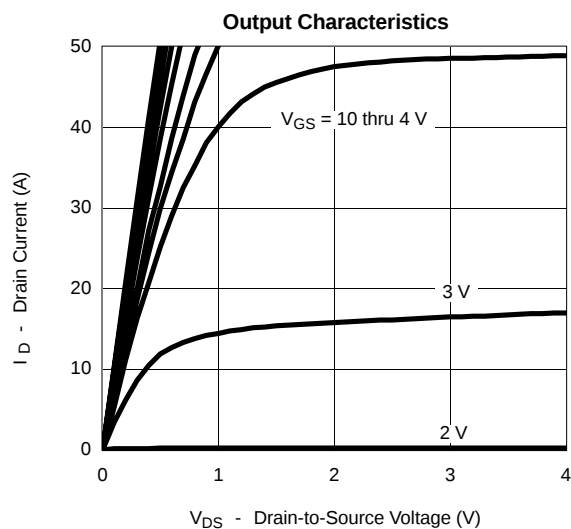
a. Surface Mounted on 1" x 1" FR4 Board.

MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.80		2	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 24\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	50			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 12.4\ \text{A}$		0.010	0.012	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 9.6\ \text{A}$		0.016	0.020	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 12.4\ \text{A}$		27		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.6\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.75	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 5.0\ \text{V}$, $I_D = 12.4\ \text{A}$		8.7	10.5	nC
Gate-Source Charge	Q_{gs}			2.4		
Gate-Drain Charge	Q_{gd}			3.5		
Gate Resistance	R_g		0.2	1	1.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \approx 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			24	50	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.6\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		50	75	

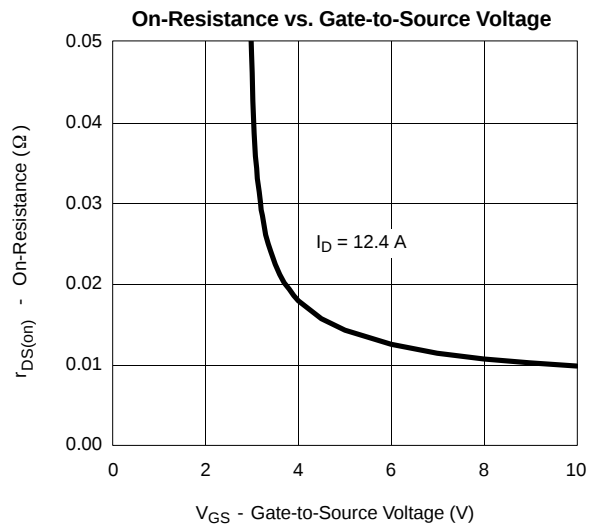
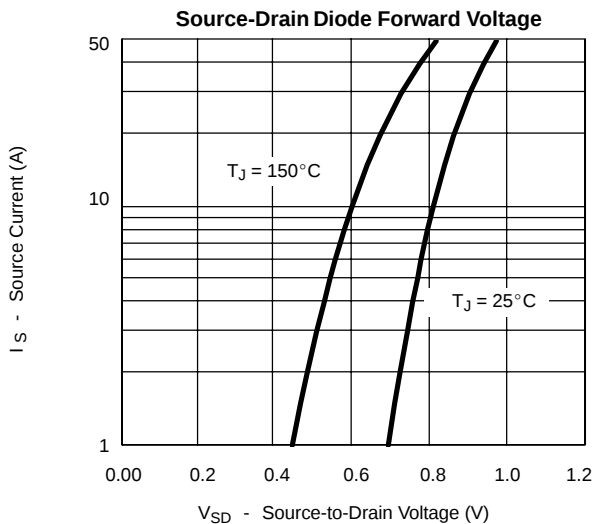
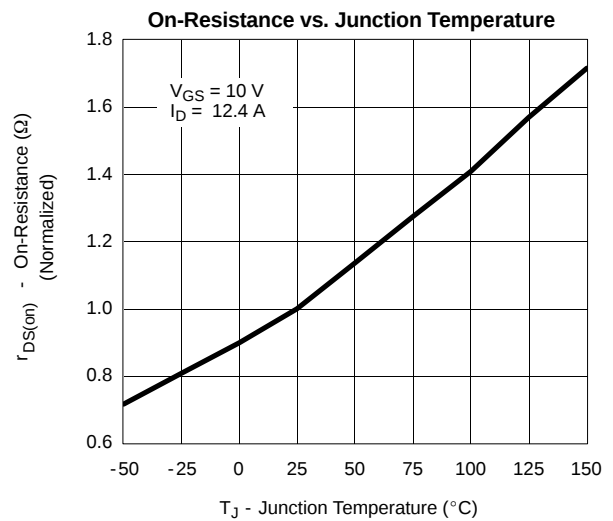
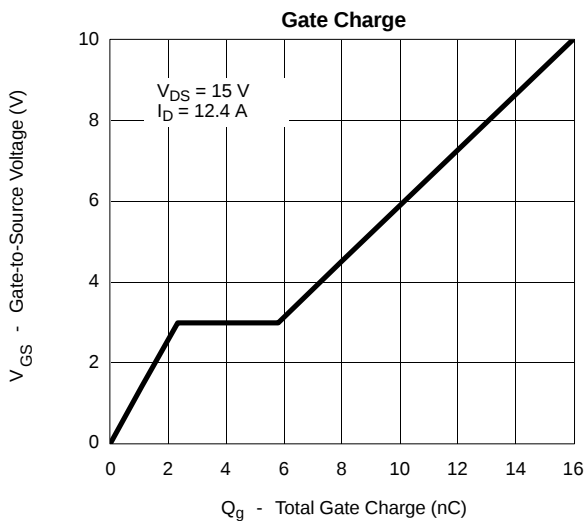
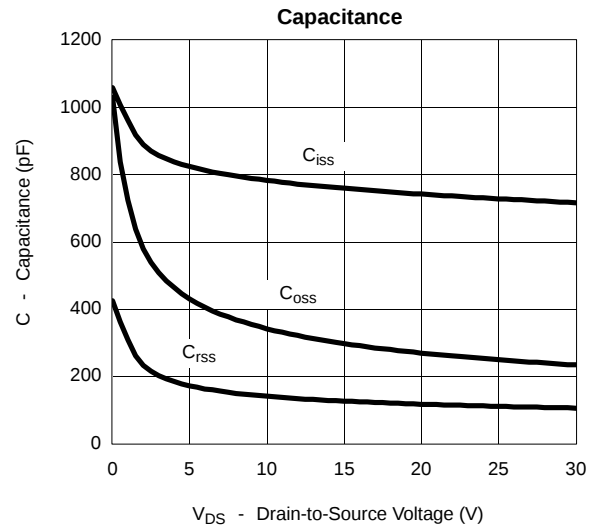
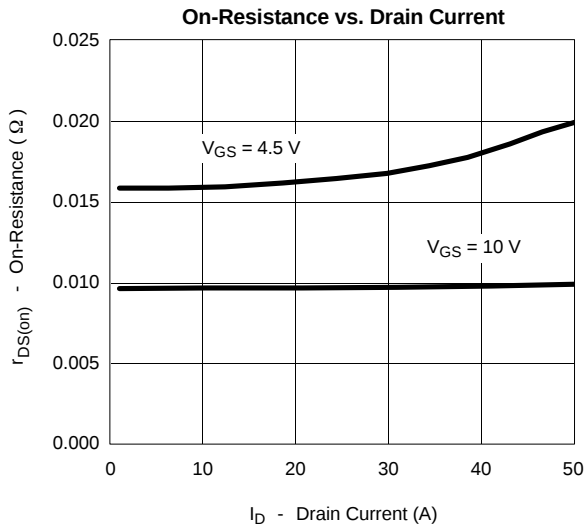
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

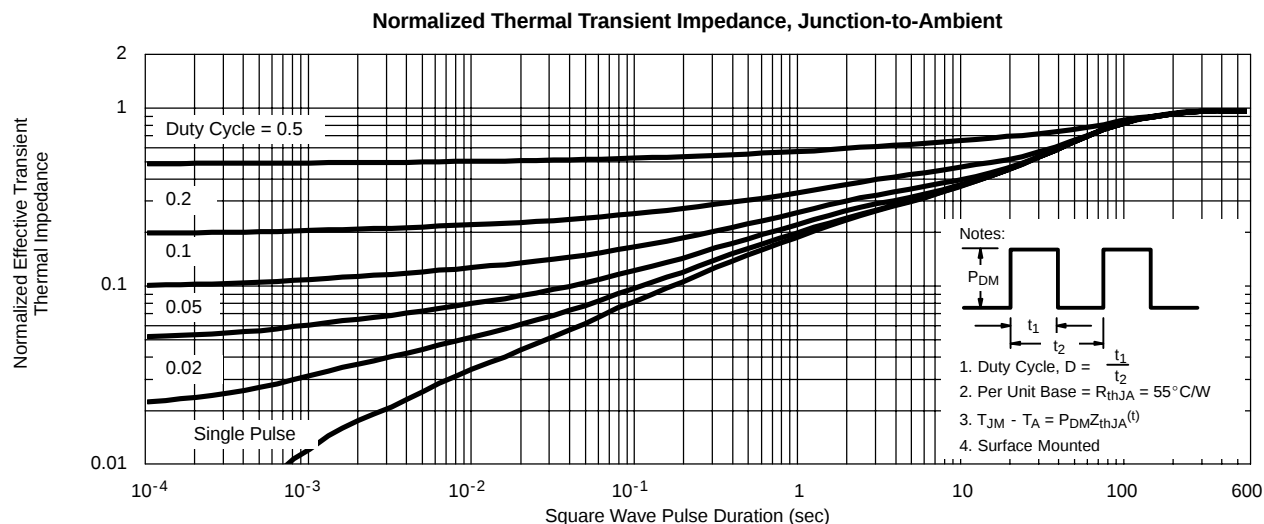
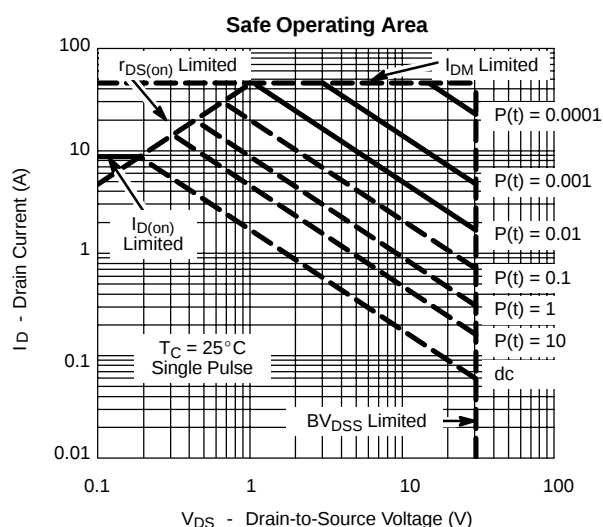
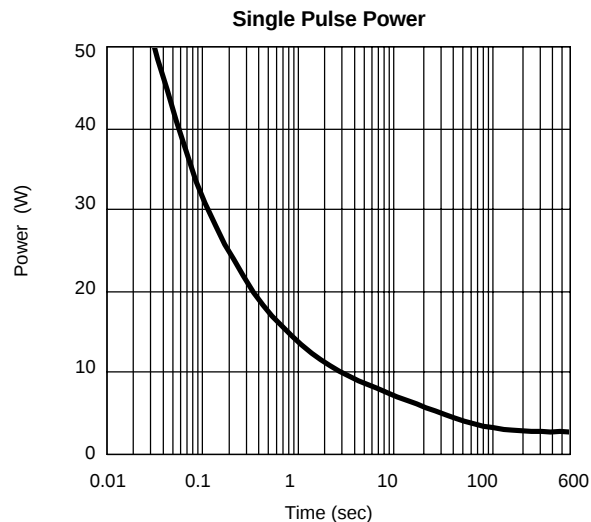
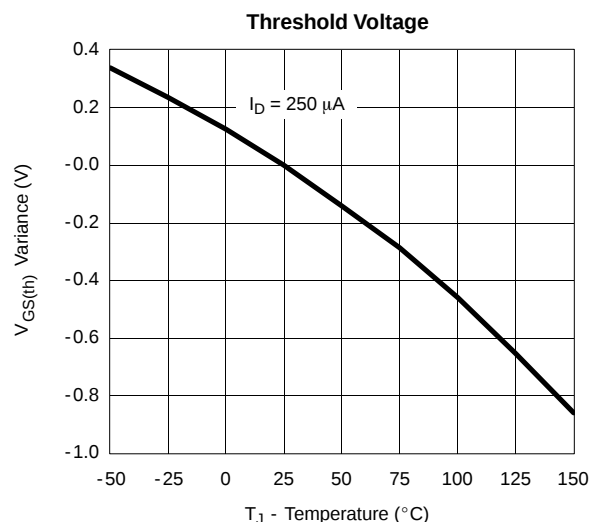
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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