High-Voltage Switchmode Controllers

FEATURES

- 10- to 120-V Input Range
- Current-Mode Control
- High-Speed, Source-Sink Output Drive
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- SHUTDOWN and RESET
- Reference Selection
  Si9110 - ±1%
  Si9111 - ±10%

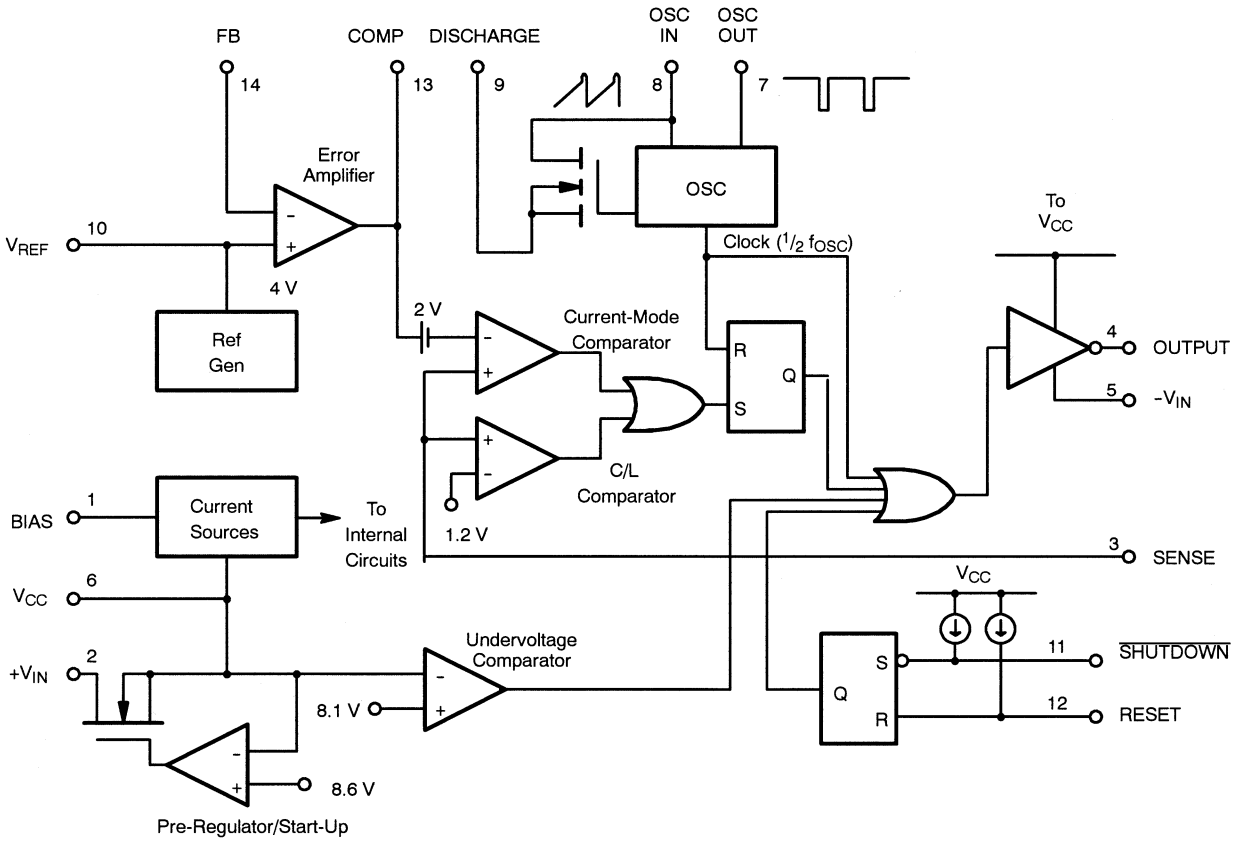
DESCRIPTION

The Si9110/9111 are BiC/DMOS integrated circuits designed for use as high-performance switchmode controllers. A high-voltage DMOS input allows the controller to work over a wide range of input voltages (10- to 120-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

A push-pull output driver provides high-speed switching for MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the Si9110/9111 can be used to implement single-ended power converter topologies (i.e., flyback, forward, and cuk).

The Si9110/9111 is available in 14-pin plastic DIP and SOIC packages, and are specified over the industrial, D suffix (-40 to 85°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)

V_{CC} . . . . . 15 V
$+V_{IN}$ . . . . . 120 V
Logic Inputs (RESET, SHUTDOWN, OSC IN, OSC OUT) . . . . . -0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SENSE, BIAS, V_{REF}) . . . . . -0.3 V to V_{CC} + 0.3 V
HV Pre-Regulator Input Current (continuous) . . . . . .5 mA
Storage Temperature . . . . . .-65 to 150°C
Operating Temperature . . . . . .-40 to 85°C
Junction Temperature (T_J) . . . . . 150°C
Power Dissipation (Package)[a]
14-Pin Plastic DIP (J Suffix)[b] . . . . . 750 mW
14-Pin SOIC (Y Suffix)[c] . . . . . 900 mW
Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP . . . . . 167°C/W
14-Pin SOIC . . . . . 140°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C.
c. Derate 7.2 mW/°C above 25°C.

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$

V_{CC} . . . . . 9.5 V to 13.5 V
$+V_{IN}$ . . . . . 10 V to 120 V
f_{OSC} . . . . . .40 kHz to 1 MHz
R_{OSC} . . . . . .25 kΩ to 1 MΩ
Linear Inputs . . . . . 0 to V_{CC} - 3 V
Digital Inputs . . . . . 0 to V_{CC}

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ		Temp[b]	D Suffix -40 to 85°C Typ[c]	Min[d]	Max[d]	Units
Reference								
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	Si9110	Room	4.0	3.92	4.08	V
			Si9111	Room	4.0	3.60	4.40	
			Si9110	Full		3.86	4.14	
			Si9111	Full		3.52	4.46	
Output Impedance[e]	Z_{OUT}			Room	30	15	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$		Room	100	70	130	µA
Temperature Stability[e]	T_{REF}			Full	0.50		1.0	mV/°C
Oscillator								
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0		Room	3	1		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k[f]		Room	100	80	120	kHz
		R_{OSC} = 150 k[f]		Room	200	160	240	
Voltage Stability	Δf/f	Δf/f=f(13.5 V) - f(9.5 V)/ f(9.5 V)		Room	10		15	%
Temperature Coefficient[e]	T_{OSC}			Full	200		500	ppm/°C

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Error Amplifier								
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = - V_{IN} (OSC Disabled)	Si9110	Room	4.00	3.96	4.04	V
			Si9111	Room	4.00	3.60	4.40	
Input BIAS Current	I_{FB}	OSC IN = - V_{IN}, V_{FB} = 4 V		Room	25		500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = - V_{IN} (OSC Disabled)		Room	±15		±40	mV
Open Loop Voltage Gain[e]	A_{VOL}			Room	80	60		dB
Unity Gain Bandwidth[e]	BW			Room	1.3	1		MHz
Dynamic Output Impedance[e]	Z_{OUT}			Room	1000		2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)		Room	-2.0		-1.4	mA
		Sink (V_{FB} = 4.5 V)		Room	0.15	0.12		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V		Room	70	50		dB
Current Limit								
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V		Room	1.2	1.0	1.4	V
Delay to Output[e]	t_d	V_{SENSE} = 1.5 V, See Figure 1.		Room	100		150	ns
Pre-Regulator/Start-Up								
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA		Room		120		V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V		Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = V_{ULVO}		Room	15	8		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA		Room	8.6	7.8	9.4	V
Undervoltage Lockout	V_{UVLO}			Room	8.1	7.0	8.9	
V_{REG} - V_{UVLO}	V_{DELTA}			Room	0.6	0.3		
Supply								
Supply Current	I_{CC}	C_{LOAD} < 75 pF (Pin 4)		Room	0.6	0.45	1.0	mA
Bias Current	I_{BIAS}			Room	15	10	20	µA
Logic								
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	C_L = 500 pF, V_{SENSE} -V_{IN} See Figure 2.		Room	50		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3.		Room		50		
RESET Pulse Width[e]	t_{RW}			Room		50		
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low[e]	t_{LW}	See Figure 3.		Room		25		
Input Low Voltage	V_{IL}			Room			2.0	V
Input High Voltage	V_{IH}			Room		8		
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V		Room	1		5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V		Room	-25	-35		

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Output							
Output High Voltage	V_{OH}	I_{OUT} = -10 mA	Room Full		9.7 9.5		V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA	Room Full			0.30 0.50	V
Output Resistance	R_{OUT}	I_{OUT} = 10 mA, Source or Sink	Room Full	20 25		30 50	Ω
Rise Time[e]	t_r	C_L = 500 pF	Room	40		75	ns
Fall Time[e]	t_f		Room	40		75	ns

Notes

a. Refer to PROCESS OPTION FLOWCHART for additional information.

b. Room = 25°C, Full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

e. Guaranteed by design, not subject to production test.

f. C_{STRAY} Pin 8 = v 5 pF.

TIMING WAVEFORMS

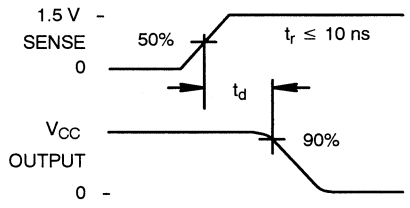


FIGURE 1.

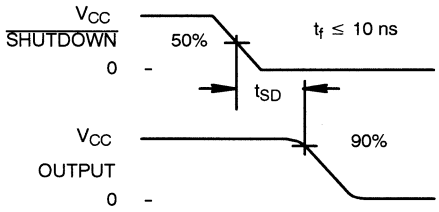


FIGURE 2.

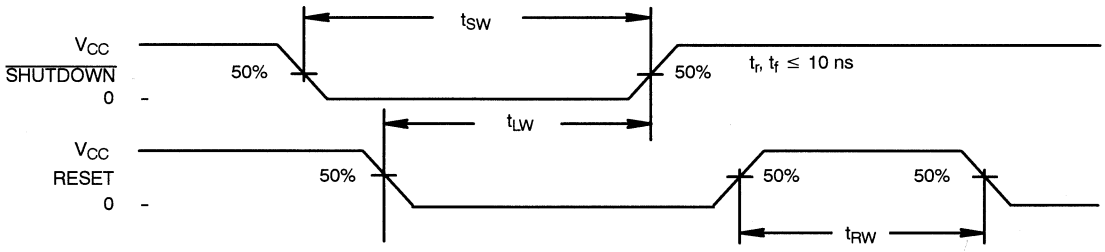


FIGURE 3.

TYPICAL CHARACTERISTICS

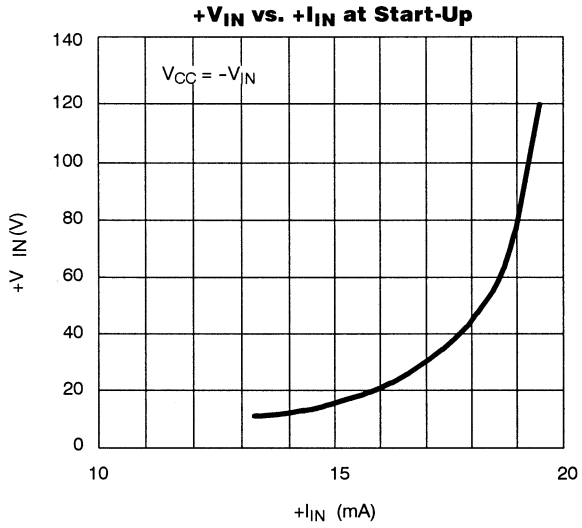


FIGURE 4.

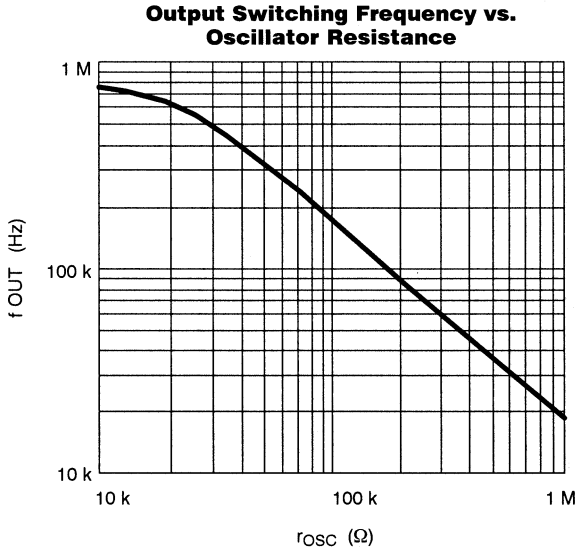
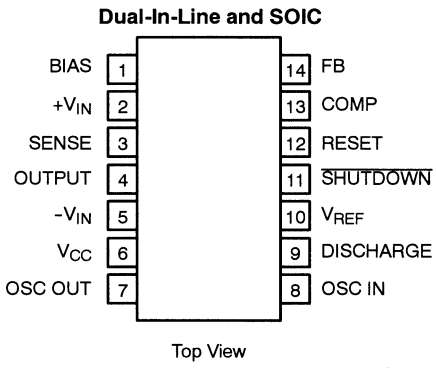


FIGURE 5.

PIN CONFIGURATIONS



Order Numbers

Plastic DIP: Si9110DJ, Si9111DJ
SOIC: Si9110DY, Si9111DY

DETAILED DESCRIPTION

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9110/9111 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary “bootstrap” winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6-V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: During start-up or when V_{CC} drops below 8.6 V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical pre-regulator current at BiC/DMOS as a function of input voltage.

BIAS

To properly set the bias for the Si9110/9111, a 390-kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15μA.

Reference Section

The reference section of the Si9110 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9110 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4 V. This compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9111 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a dc bias point for the error amplifier.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with “around-the-amplifier” compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN (pin 8) terminal. For a 5-V pulse amplitude and 0.5-μs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

TABLE 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H		Normal Operation (No Change)
L	H	Off (Not Latched)