



P-Channel 50-V (D-S) MOSFET

CHARACTERISTICS

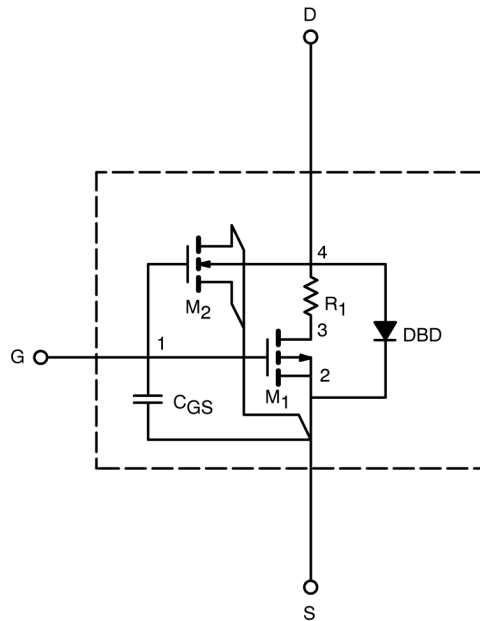
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model schematic is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Condition	Typical	Unit
Static				
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	1.82	V
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	61	A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -10 V, I _D = -3.5 A	0.08	Ω
		V _{GS} = -4.5 V, I _D = -3.1 A	0.10	
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -3.5A	7.2	S
Diode Forward Voltage ^a	V _{SD}	I _S = -2.5A, V _{GS} = 0 V	-0.82	V
Dynamic^b				
Total Gate Charge ^b	Q _g	V _{DS} = -30V, V _{GS} = -10V, I _D = -3.5A	17	nC
Gate-Source Charge ^b	Q _{gs}		5	
Gate-Drain Charge ^b	Q _{gd}		2	
Turn-On Delay Time ^b	t _{d(on)}	V _{DD} = -30V, R _L = 30Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6Ω	4	ns
Rise Time ^b	t _r		4.1	
Turn-Off Delay Time ^b	t _{d(off)}		23	
Fall Time ^b	t _f		14	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -2.5 A, di/dt = 100 A/μs	

Notes

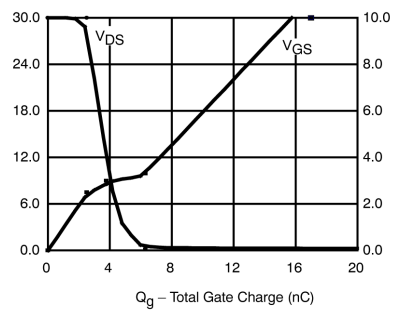
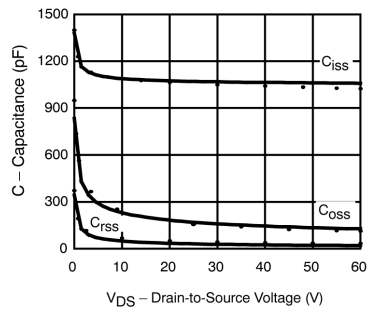
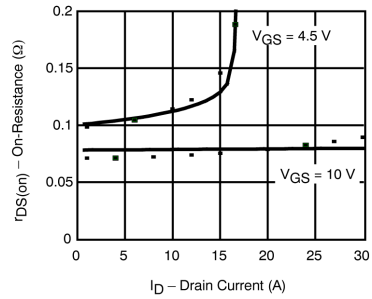
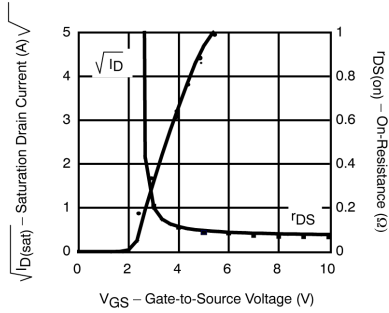
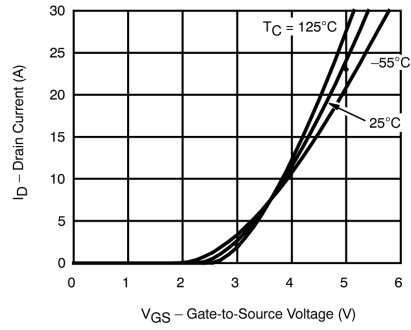
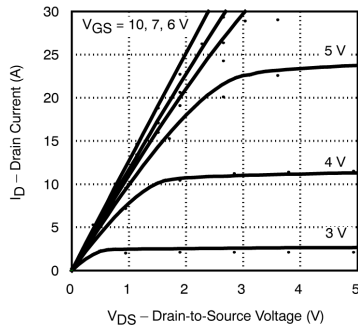
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by desing, not subject to production testing.



SPICE Device Model Si9407AEY

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.