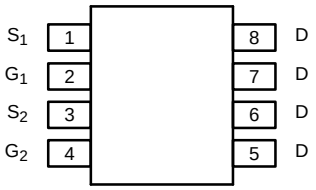
# N-/P-Channel, Reduced $Q_g$, Fast Switching Half-Bridge

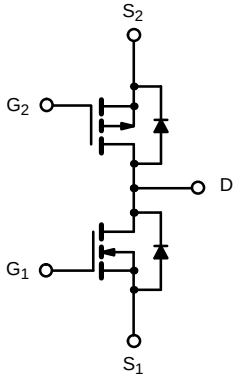
**High-Efficiency PWM Optimized**

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| | $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
| N-Channel | 20 | 0.055 @ $V_{GS}$ = 4.5 V | ±4.5 |
| | | 0.075 @ $V_{GS}$ = 3.0 V | ±3.8 |
| P-Channel | –20 | 0.080 @ $V_{GS}$ = –4.5 V | ±4.0 |
| | | 0.120 @ $V_{GS}$ = –3.0 V | ±3.0 |

**SO-8**




Top View




| ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|---|---|---|---|---|
| Parameter | | Symbol | N-Channel | P-Channel | Unit |
| Drain-Source Voltage | | $V_{DS}$ | 20 | –20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±14 | | |
| Continuous Drain Current ($T_J$ = 150°C)[a] | $T_A$ = 25°C | $I_D$ | ±4.5 | ±4.0 | A |
| | $T_A$ = 70°C | | ±3.6 | ±3.0 | |
| Pulsed Drain Current | | $I_{DM}$ | ±20 | | |
| Continuous Source Current (Diode Conduction)[a] | | $I_S$ | 1.7 | –1.7 | |
| Maximum Power Dissipation[a] | $T_A$ = 25°C | $P_D$ | 2.0 | | W |
| | $T_A$ = 70°C | | 1.3 | | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | –55 to 150 | | °C |

| THERMAL RESISTANCE RATINGS | | | |
|---|---|---|---|
| Parameter | Symbol | N- or P-Channel | Unit |
| Maximum Junction-to-Ambient[a] | $R_{thJA}$ | 62.5 | °C/W |

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

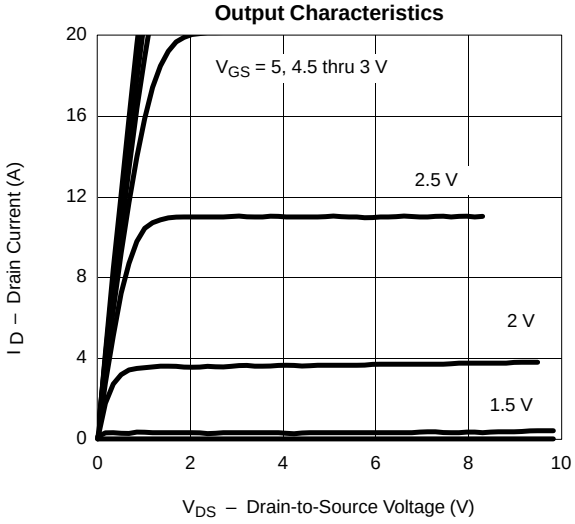
## SPECIFICATIONS ($T_J$ = 25°C UNLESS OTHERWISE NOTED)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static** | | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | N-Ch | 0.6 | | | V |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | P-Ch | –0.6 | | | |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±12 V | N-Ch | | | ±100 | nA |
| | | | P-Ch | | | ±100 | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | N-Ch | | | 1 | μA |
| | | $V_{DS}$ = –20 V, $V_{GS}$ = 0 V | P-Ch | | | –1 | |
| | | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, $T_J$ = 70°C | N-Ch | | | 25 | |
| | | $V_{DS}$ = –20 V, $V_{GS}$ = 0 V, $T_J$ = 70°C | P-Ch | | | –25 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ = 5 V, $V_{GS}$ = 4.5 V | N-Ch | 20 | | | A |
| | | $V_{DS}$ = –5 V, $V_{GS}$ = –4.5 V | P-Ch | –20 | | | |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 4.5 A | N-Ch | | 0.044 | 0.055 | Ω |
| | | $V_{GS}$ = –4.5 V, $I_D$ = –4.0 A | P-Ch | | 0.064 | 0.080 | |
| | | $V_{GS}$ = 3.0 V, $I_D$ = 3.8 A | N-Ch | | 0.055 | 0.075 | |
| | | $V_{GS}$ = –3.0 V, $I_D$ = –3.0 A | P-Ch | | 0.086 | 0.120 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 4.5 A | N-Ch | | 11.5 | | S |
| | | $V_{DS}$ = –15 V, $I_D$ = –4.0 A | P-Ch | | 9.8 | | |
| Diode Forward Voltage[a] | $V_{SD}$ | $I_S$ = 1.7 A, $V_{GS}$ = 0 V | N-Ch | | 0.73 | 1.2 | V |
| | | $I_S$ = –1.7 A, $V_{GS}$ = 0 V | P-Ch | | –0.75 | –1.2 | |
| **Dynamic[b]** | | | | | | | |
| Total Gate Charge | $Q_g$ | N-Channel $V_{DS}$ = 3.5 V, $V_{GS}$ = 4.5 V, $I_D$ = 0.8 A<br>P-Channel $V_{DS}$ = –3.5 V, $V_{GS}$ = –4.5 V $I_D$ = –0.8 A | N-Ch | | 5.2 | 10 | nC |
| | | | P-Ch | | 7.9 | 15 | |
| Gate-Source Charge | $Q_{gs}$ | | N-Ch | | 0.95 | | |
| | | | P-Ch | | 1.60 | | |
| Gate-Drain Charge | $Q_{gd}$ | | N-Ch | | 1.15 | | |
| | | | P-Ch | | 1.90 | | |
| Turn-On Delay Time | $t_{d(on)}$ | N-Channel $V_{DD}$ = 3.5 V, $R_L$ = 4.3 Ω $I_D$ ≅ 0.8 A, $V_{GEN}$ = 4.5 V, $R_G$ = 6 Ω<br>P-Channel $V_{DD}$ = –3.5 V, $R_L$ = 4.3 Ω $I_D$ ≅ –0.8 A, $V_{GEN}$ = –4.5 V, $R_G$ = 6 Ω | N-Ch | | 12 | 20 | ns |
| | | | P-Ch | | 20 | 40 | |
| Rise Time | $t_r$ | | N-Ch | | 22 | 50 | |
| | | | P-Ch | | 52 | 90 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | N-Ch | | 27 | 50 | |
| | | | P-Ch | | 37 | 60 | |
| Fall Time | $t_f$ | | N-Ch | | 8 | 20 | |
| | | | P-Ch | | 11 | 20 | |
| Source-Drain Reverse Recovery Time | $t_{rr}$ | N-Channel—$I_F$ = 1.7 A, di/dt = 100 A/μs | N-Ch | | 60 | 100 | |
| | | P-Channel—$I_F$ = –1.7 A, di/dt = 100 A/μs | P-Ch | | 60 | 100 | |

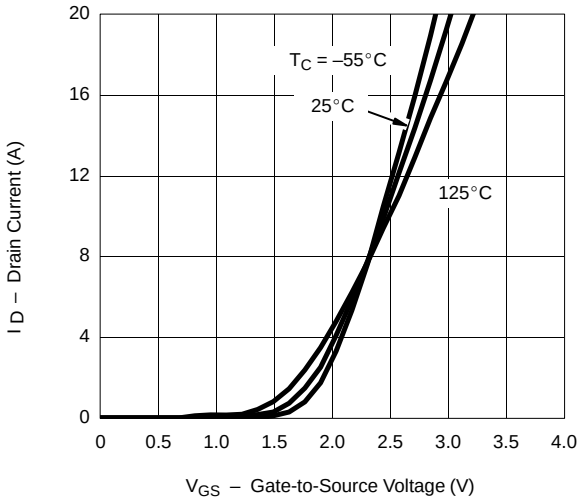
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL

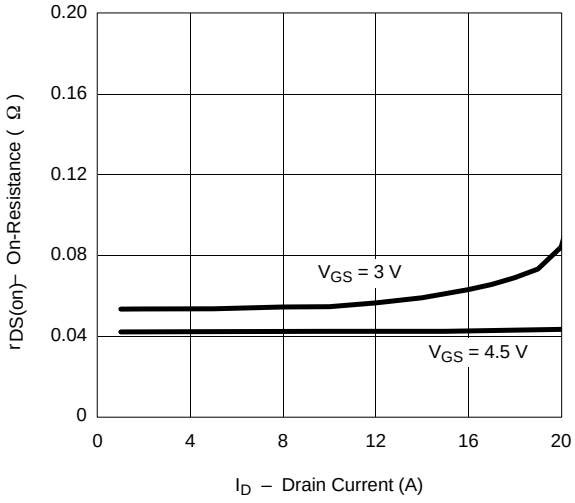
**Output Characteristics**



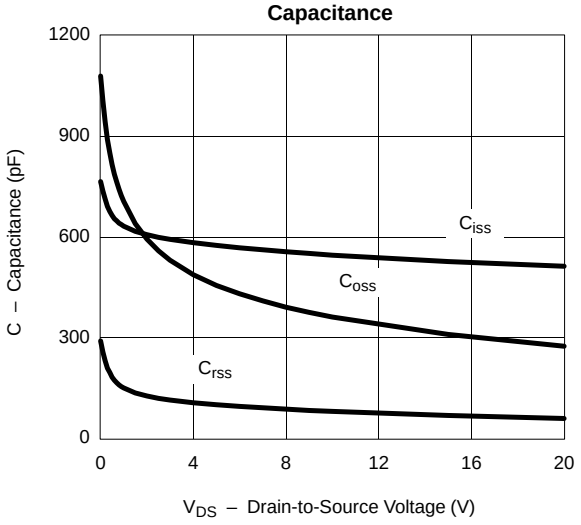

**Transfer Characteristics**



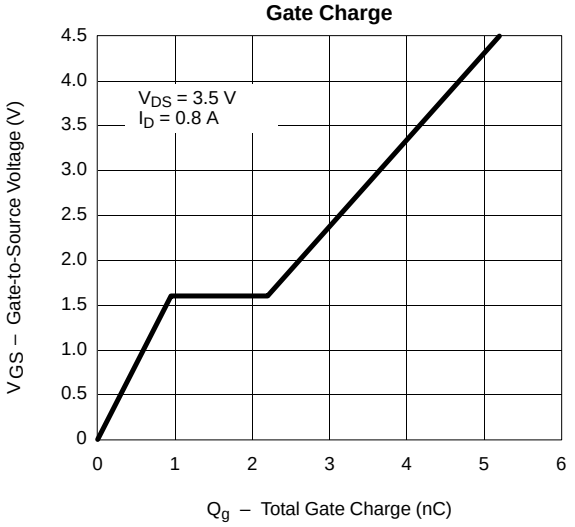

**On-Resistance vs. Drain Current**



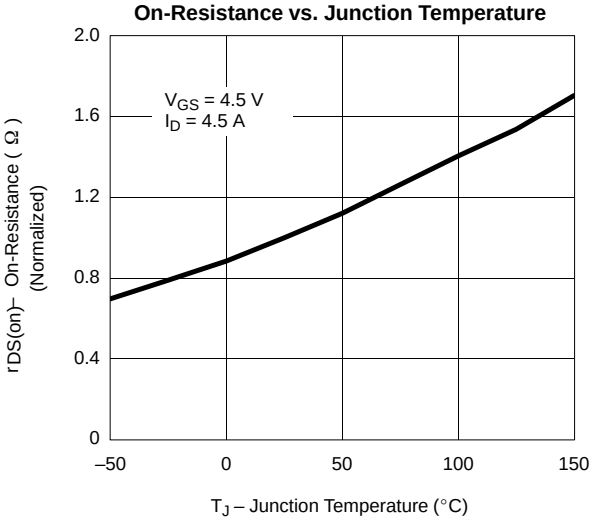

**Capacitance**




**Gate Charge**

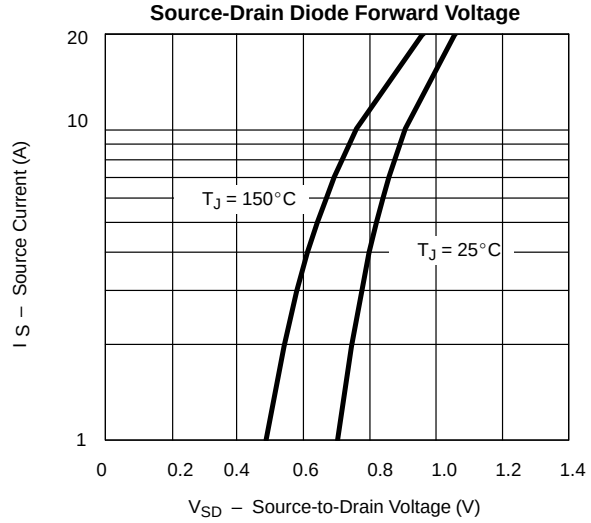



**On-Resistance vs. Junction Temperature**

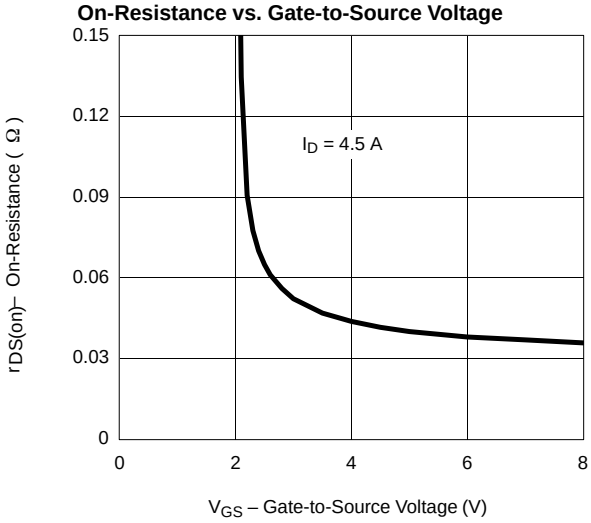


## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL

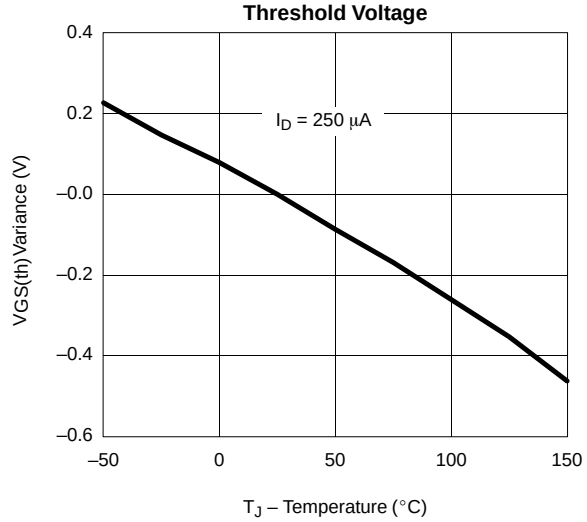
**Source-Drain Diode Forward Voltage**



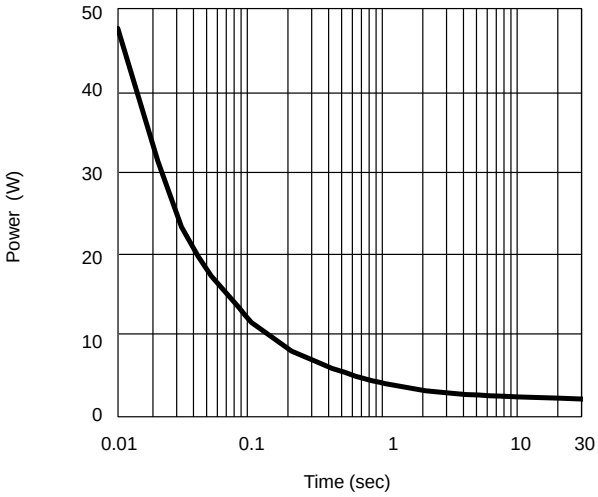

**On-Resistance vs. Gate-to-Source Voltage**



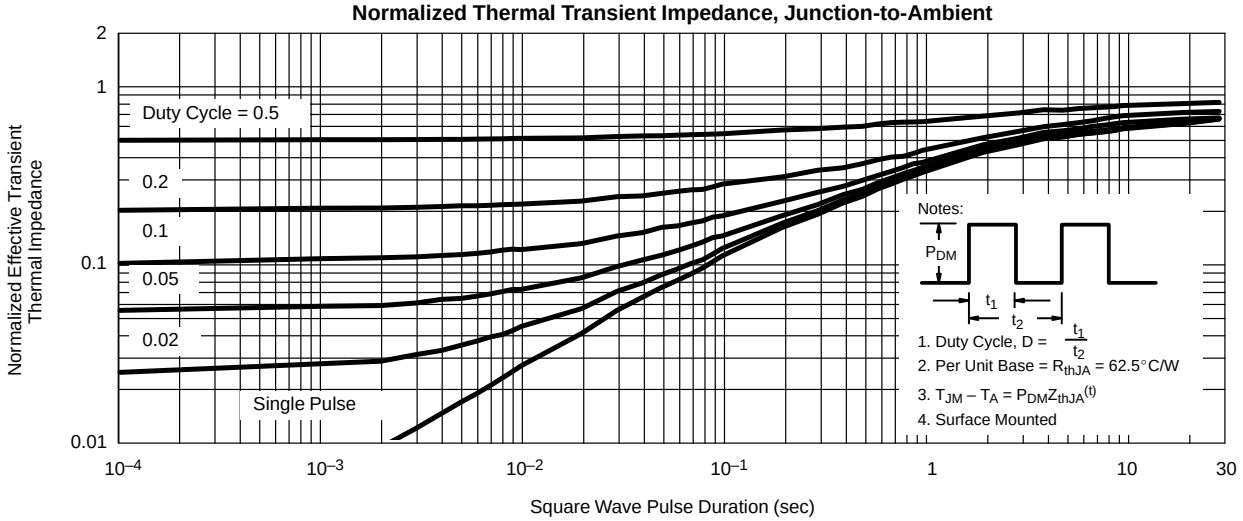

**Threshold Voltage**




**Single Pulse Power**

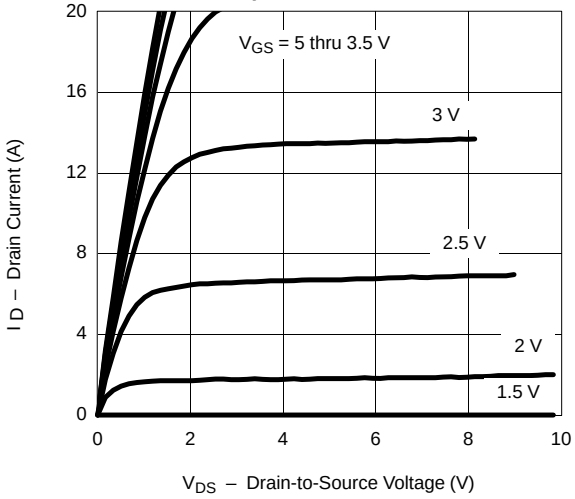



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

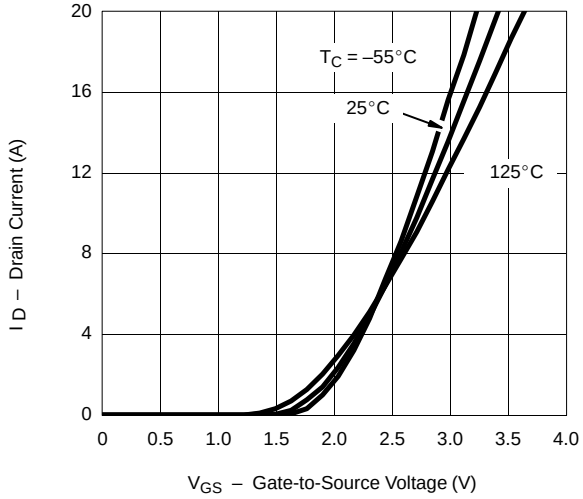


## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

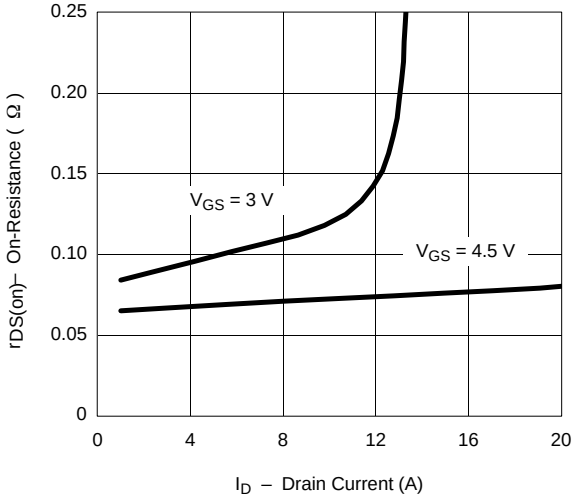
**Output Characteristics**



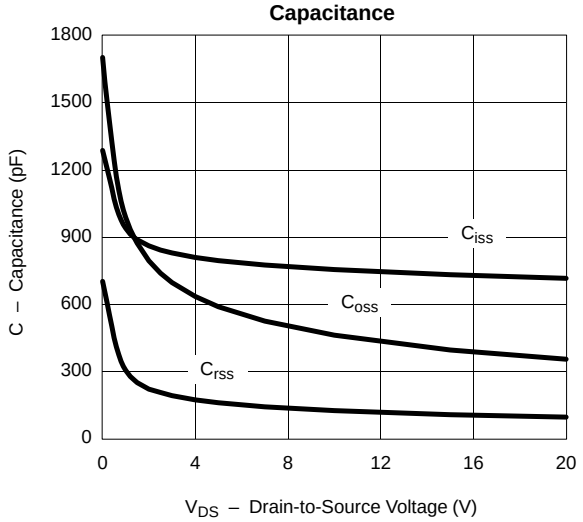

**Transfer Characteristics**



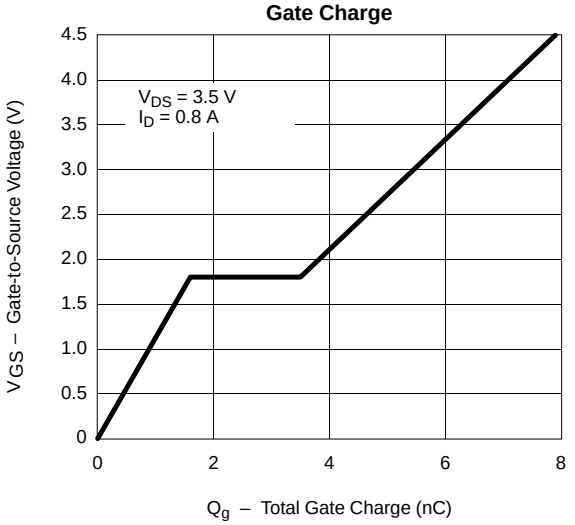

**On-Resistance vs. Drain Current**




**Capacitance**




**Gate Charge**

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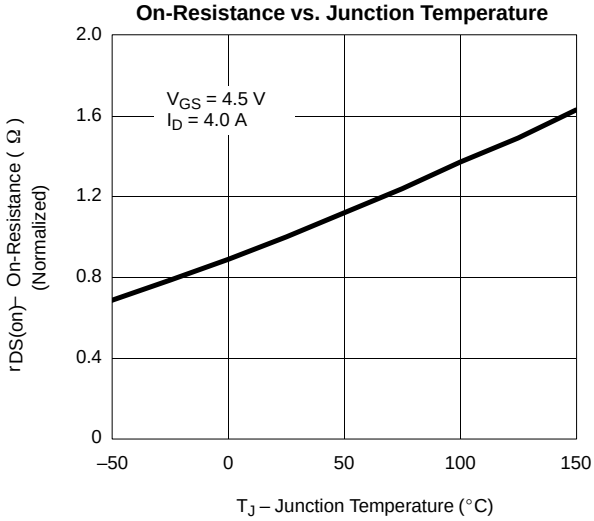

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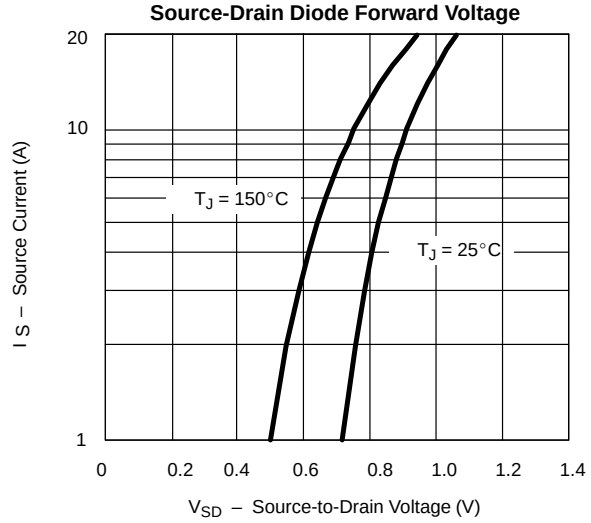
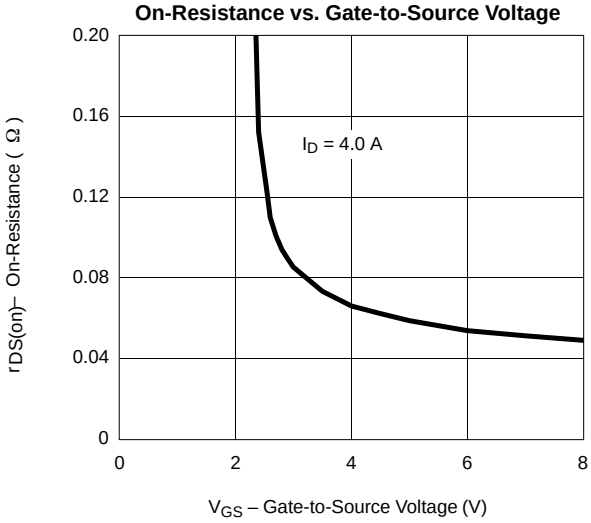
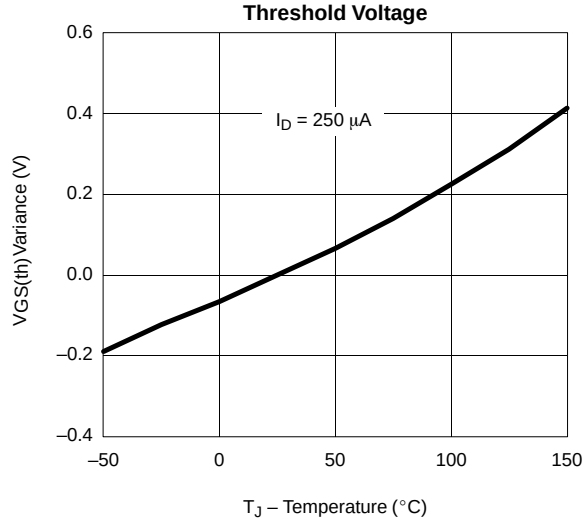



**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**

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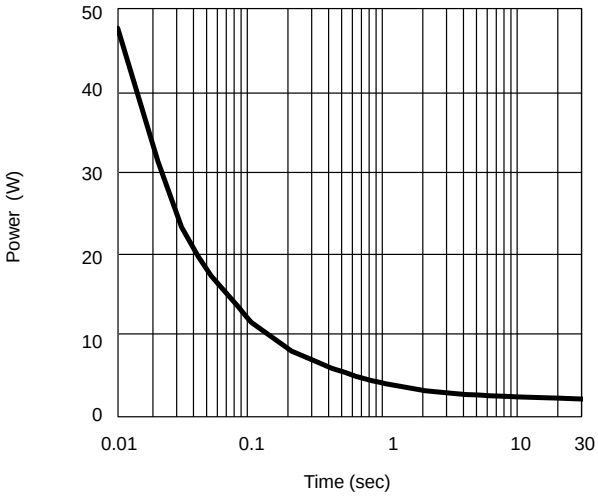


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