

## N- and P-Channel 20-V (D-S) MOSFET

### CHARACTERISTICS

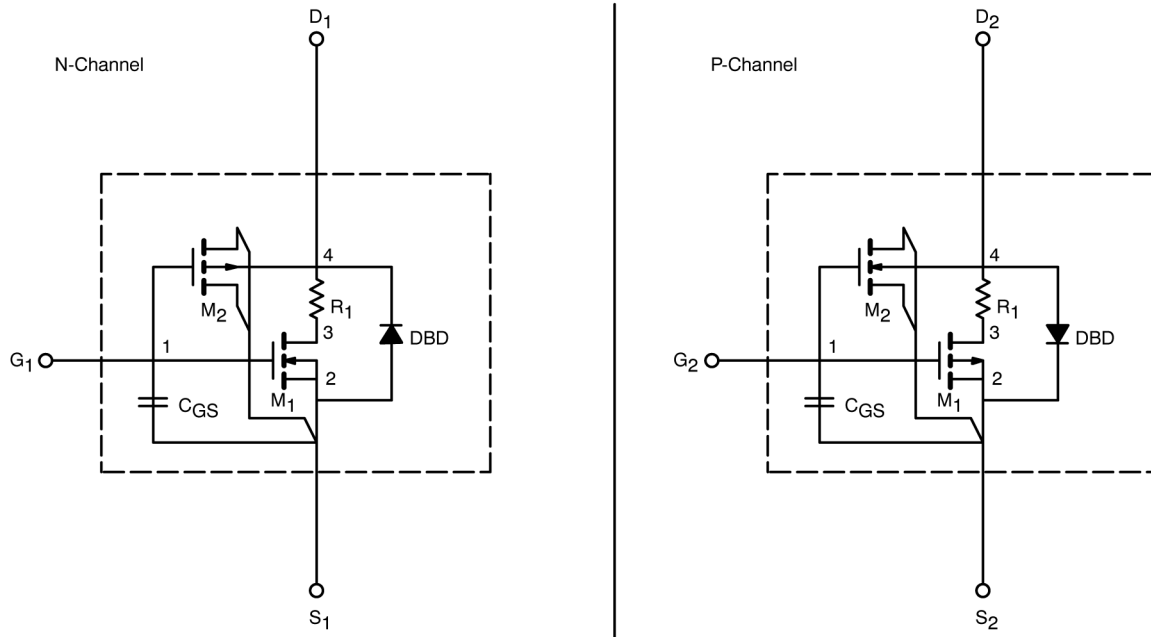
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the  $-55$  to  $125^{\circ}\text{C}$  Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The model subcircuit schematic is extracted and optimized over the  $-55$  to  $125^{\circ}\text{C}$  temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SPICE Device Model 9928DY

Vishay Siliconix



SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Condition	Typical <sup>a</sup>	Unit
<b>Static</b>				
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V, V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	
		V <sub>DS</sub> = V, V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = V, V <sub>GS</sub> = V	N-Ch	
		V <sub>DS</sub> = -V, V <sub>GS</sub> = -V	P-Ch	
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A	N-Ch	0.044
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.2 A	P-Ch	.056
		V <sub>GS</sub> = 3.0 V, I <sub>D</sub> = 3.9 A	N-Ch	0.051
		V <sub>GS</sub> = -3.0 V, I <sub>D</sub> = -2.0 A	P-Ch	0.084
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 1 A	P-Ch	0.056
		V <sub>GS</sub> = -2.7 V, I <sub>D</sub> = -1 A	P-Ch	0.096
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 A	N-Ch	15
		V <sub>DS</sub> = -9 V, I <sub>D</sub> = -3.4 A	P-Ch	9.3
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	N-Ch	0.84
		I <sub>S</sub> = -2 V, V <sub>GS</sub> = 0 V	P-Ch	-0.74
<b>Dynamic<sup>a</sup></b>				
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 6 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A P-Channel V <sub>DS</sub> = -6 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.2 A	N-Ch	8
Gate-Source Charge	Q <sub>gs</sub>		P-Ch	8.9
			N-Ch	2
Gate-Drain Charge	Q <sub>gd</sub>		P-Ch	2.1
			N-Ch	2.4
Turn-On Delay Time	t <sub>d(on)</sub>		P-Ch	3.3
		N-Ch	24	
Rise Time	t <sub>r</sub>	P-Ch	12	
		N-Ch	19	
Turn-Off Delay Time	t <sub>d(off)</sub>	P-Ch	19	
		N-Ch	30	
Fall Time	t <sub>f</sub>	P-Ch	46	
		N-Ch	13	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	P-Ch	60	
		N-Ch	64	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = A, I <sub>S</sub> = 1.25A, di/dt = 100 A/μs	P-Ch	53

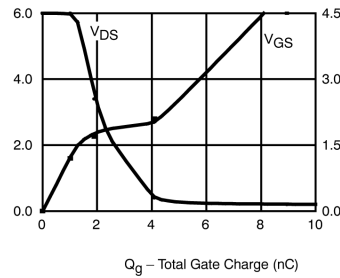
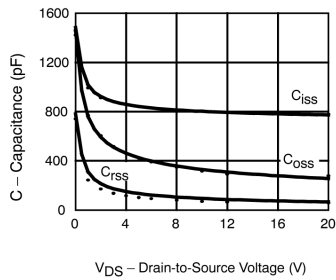
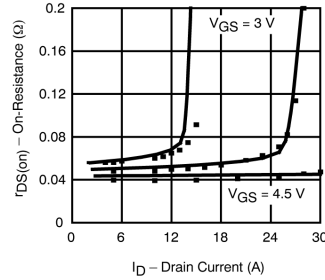
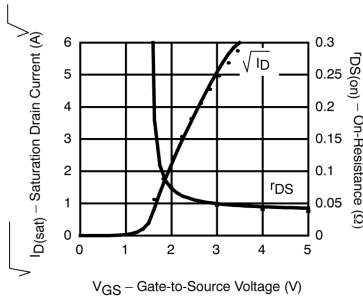
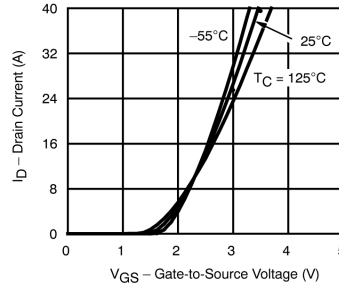
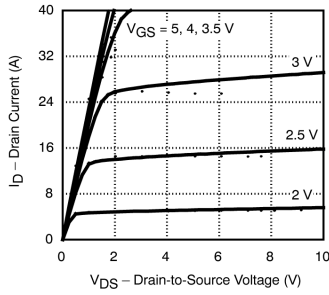
**Notes**

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



**COMPARISON OF MODEL WITH MEASURED DATA (T<sub>J</sub>=25°C UNLESS OTHERWISE NOTED)**

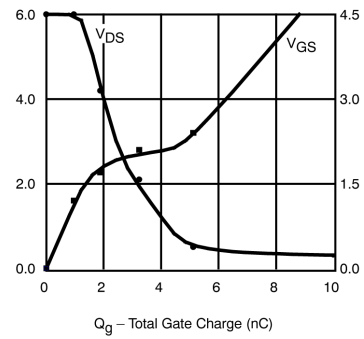
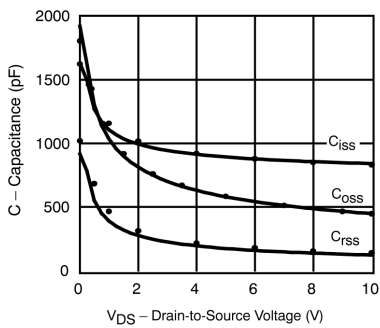
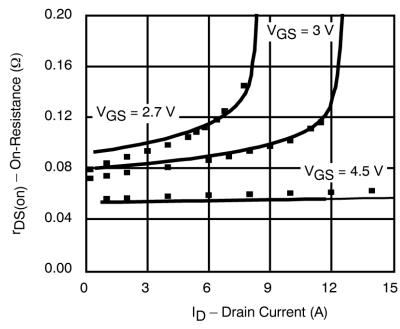
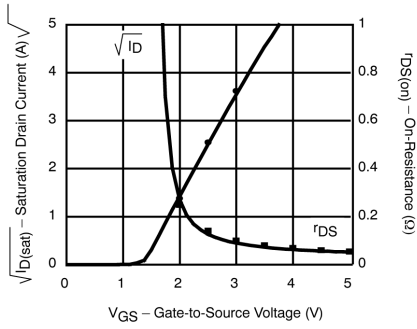
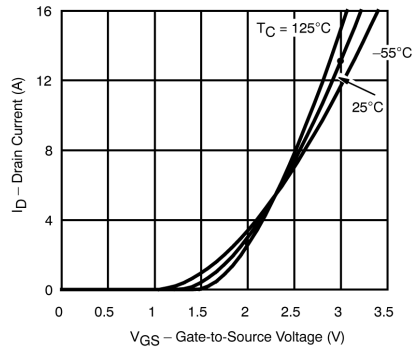
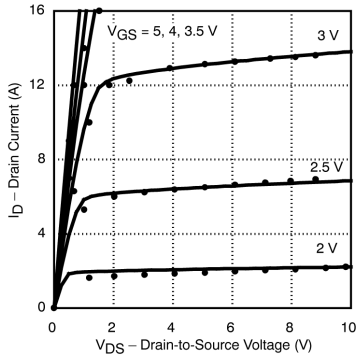
*N-Channel*



Note: Dots and squares represent measured data.



P-Channel



Note: Dots and squares represent measured data.