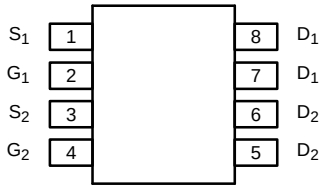
Dual P-Channel 2.5-V (G-S) MOSFET

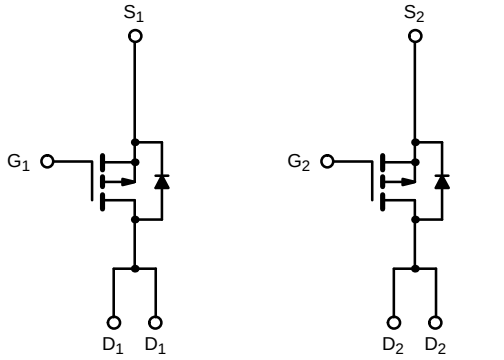
2.5-V Rated

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–12	0.05 @ V_{GS} = –4.5 V	±5
	0.074 @ V_{GS} = –2.5 V	±4.1

SO-8



Top View



P-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	–12	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±5	A
	T_A = 70°C		±4.0	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Limit**	**Unit**
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm

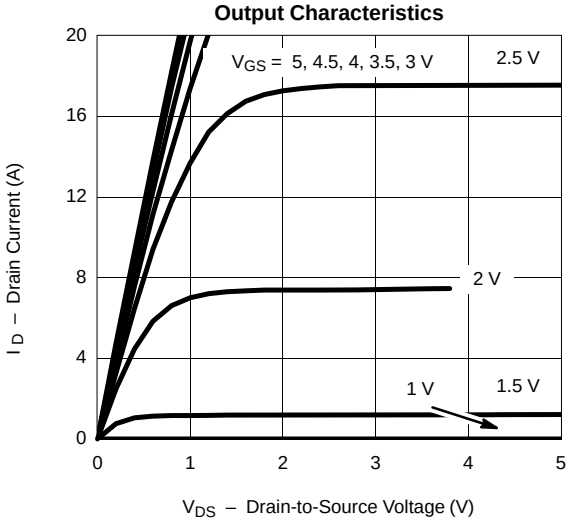
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static–0.6						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250 μA	–0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –12 V, V_{GS} = 0 V			–1	μA
		V_{DS} = –12 V, V_{GS} = 0 V, T_J = 55°C			–5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = –4.5 V	–20			A
		V_{DS} ≥ 5 V, V_{GS} = –2.5 V	–6			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = –5 A		0.039	0.05	Ω
		V_{GS} = –2.5 V, I_D = –3 A		0.051	0.074	
Forward Transconductance[b]	g_{fs}	V_{DS} = –9 V, I_D = –5 A		16		S
Diode Forward Voltage[b]	V_{SD}	I_S = –1.7 A, V_{GS} = 0 V		–0.75	–1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –5 A		21	40	nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –6 V, R_L = 6 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω		20	40	ns
Rise Time	t_r			40	80	
Turn-Off Delay Time	$t_{d(off)}$			100	200	
Fall Time	t_f			60	120	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –1.7 A, di/dt = 100 A/μs		67	100	

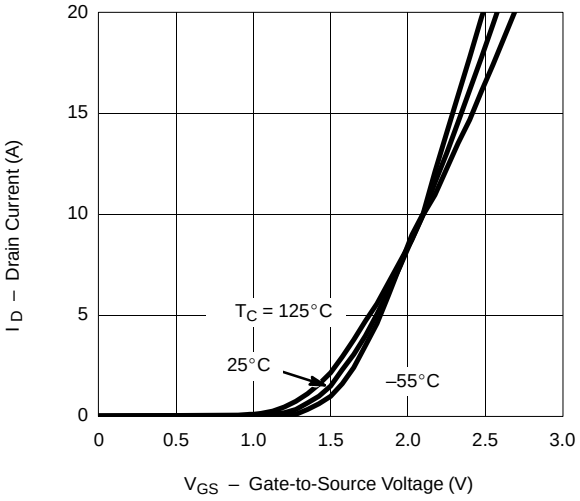
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

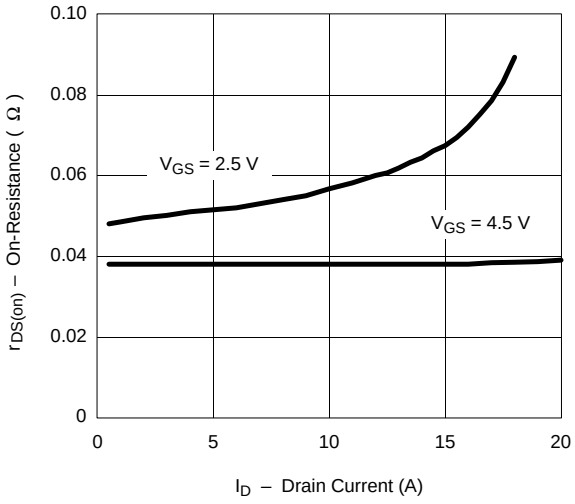
Output Characteristics



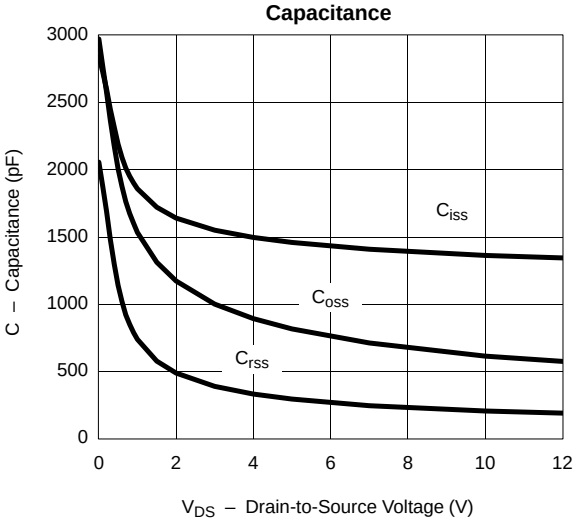
Transfer Characteristics



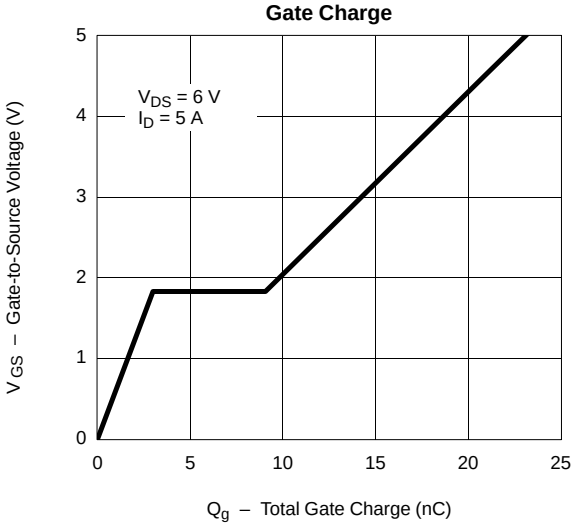
On-Resistance vs. Drain Current



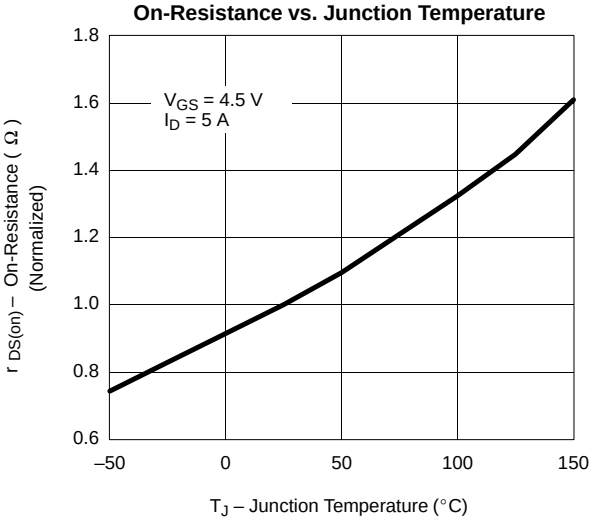
Capacitance



Gate Charge

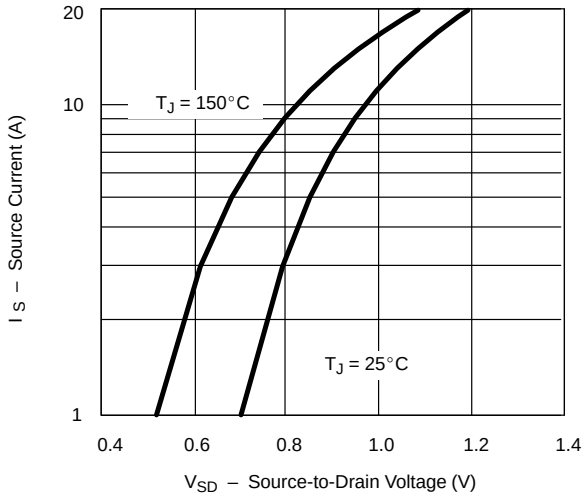


On-Resistance vs. Junction Temperature

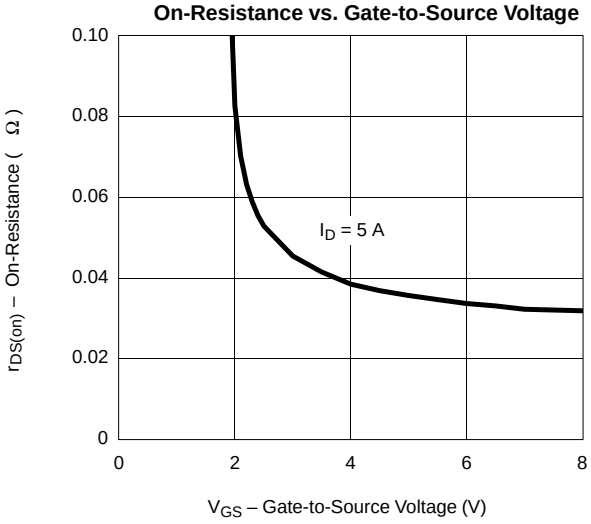


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

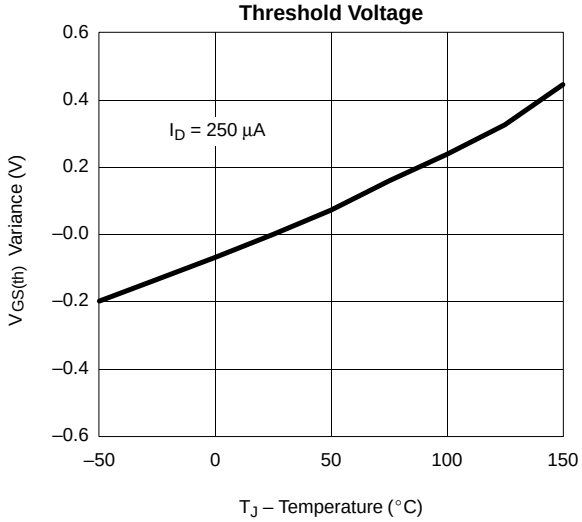
Source-Drain Diode Forward Voltage



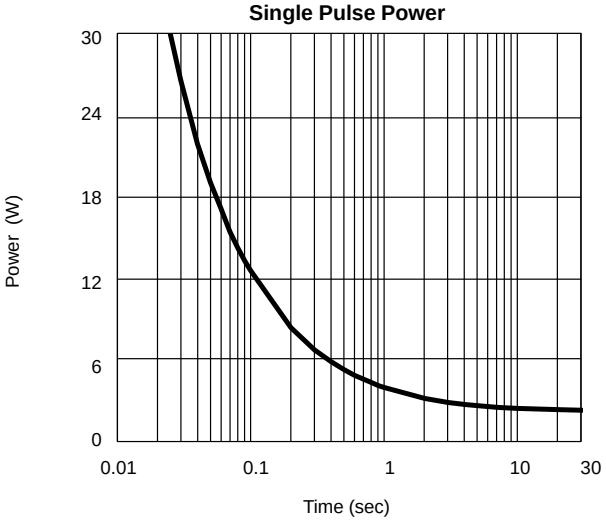
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient