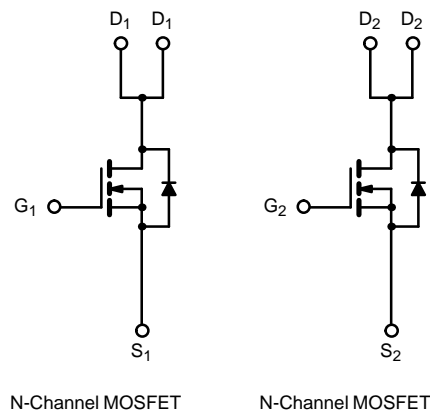
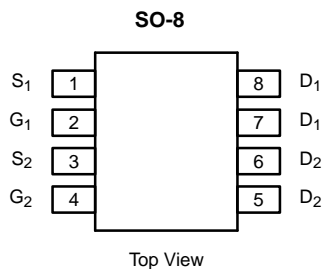




## Dual N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
30	0.050 @ $V_{GS} = 10$ V	$\pm 5.0$
	0.080 @ $V_{GS} = 4.5$ V	$\pm 3.9$



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	$\pm 5.0$
		$T_A = 70^\circ\text{C}$	$\pm 4.0$
Pulsed Drain Current	$I_{DM}$	$\pm 40$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.7	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	2
		$T_A = 70^\circ\text{C}$	1.3
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

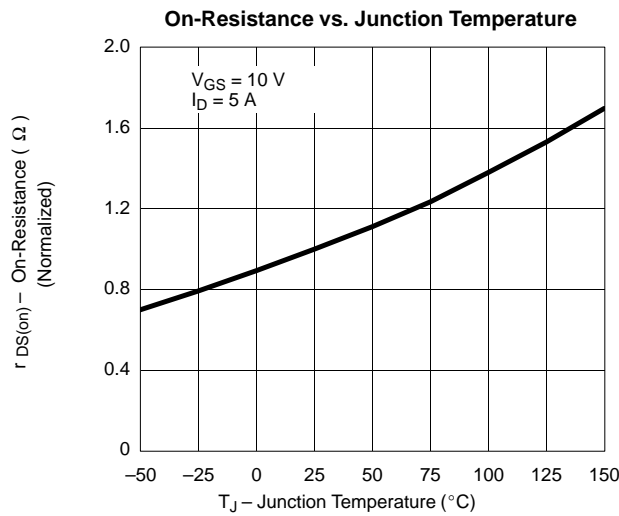
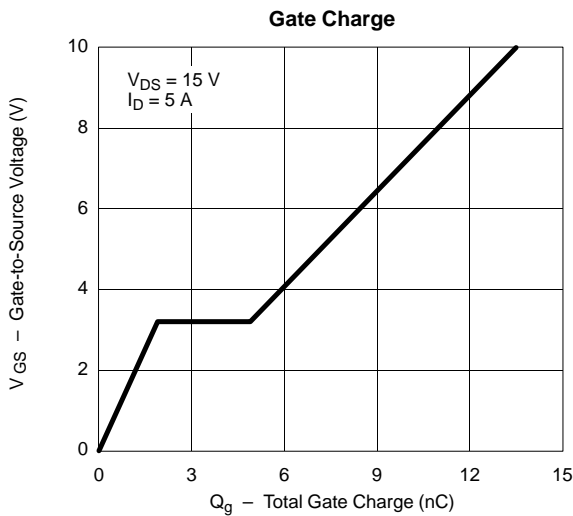
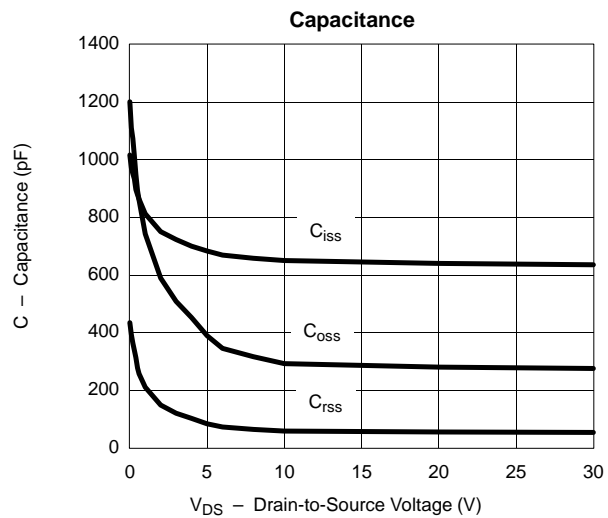
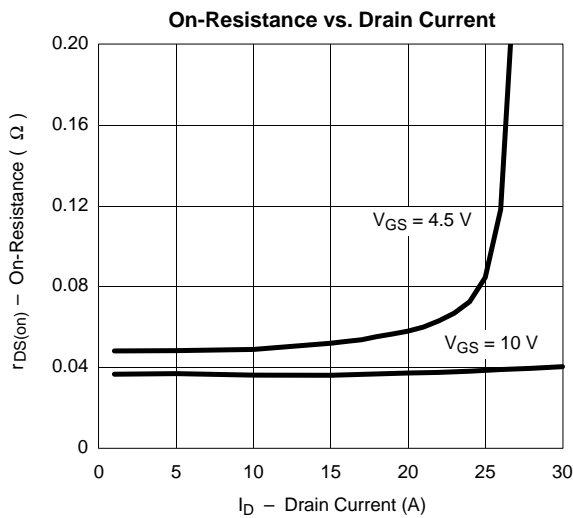
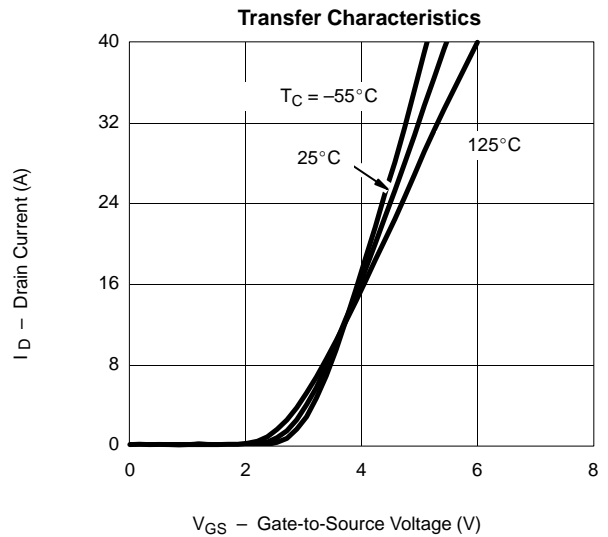
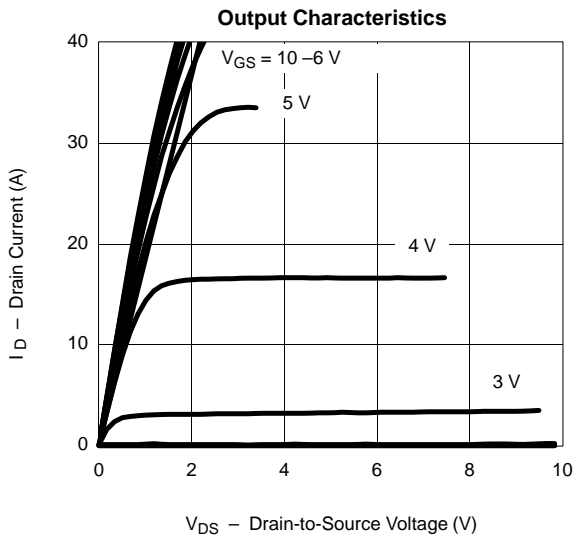


<b>SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)</b>						
Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			2	μA
		V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			20	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	40			A
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.0 A		0.039	0.050	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.9 A		0.052	0.080	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5.0 A		10		S
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.7 A, V <sub>GS</sub> = 0 V		0.72	1.2	V
<b>Dynamic<sup>a</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.0 A		13.5	35	nC
Gate-Source Charge	Q <sub>GS</sub>			1.9		
Gate-Drain Charge	Q <sub>gd</sub>			3		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		11	30	ns
Rise Time	t <sub>r</sub>			9	25	
Turn-Off Delay Time	t <sub>d(off)</sub>			25	50	
Fall Time	t <sub>f</sub>			10	50	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 5.0 A, di/dt = 100 A/μs		60	160	

Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

