



Monolithic N-Channel JFET Duals

SST404NL
SST406NLU401NL
U404NL

U406NL

PRODUCT SUMMARY

Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Typ (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
U401NL	-0.5 to -2.5	-40	1	-2	5
SST/U404NL	-0.5 to -2.5	-40	1	-2	15
SST/U406NL	-0.5 to -2.5	-40	1	-2	40

FEATURES

- Anti Latchup Capability
- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 2 pA
- Low Noise
- High CMRR: 102 dB

BENEFITS

- External Substrate Bias—Avoids Latchup
- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

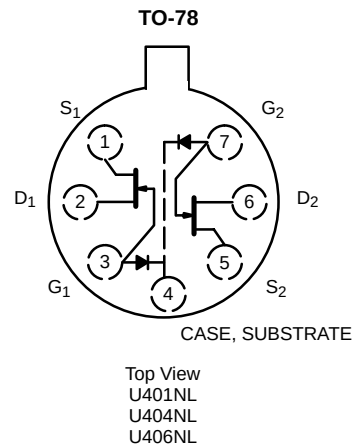
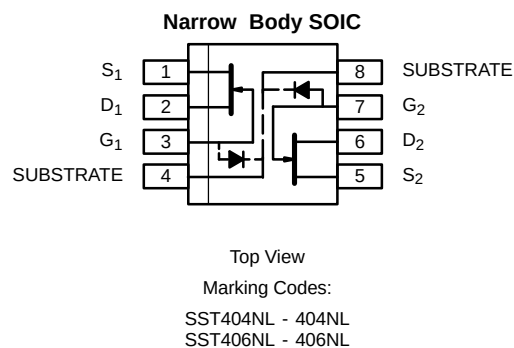
DESCRIPTION

The SST/U401NL series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. This series has a wide selection of offset and drift specifications with the U401NL featuring a 5-mV offset and 10- μ V/ $^{\circ}$ C drift.

Pins 4 and 8 of the SST series, and pin 4 of the U series part

numbers enable the substrate to be connected to a positive polarity, external bias (V_{DD}) to avoid latchup.

The U series, hermetically sealed TO-78 package is available with full military processing. The SST series SO-8 package provides ease of manufacturing, and the symmetrical pinout prevents improper orientation. The SO-8 package is available with tape-and-reel options for compatibility with automatic assembly methods.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage -40 V
Gate Current 10 mA
Lead Temperature ($1/16$ " from case for 10 sec.) 300 $^{\circ}$ C
Storage Temperature : U Prefix -65 to 200 $^{\circ}$ C
SST Prefix -55 to 150 $^{\circ}$ C
For applications information see AN106.

Operating Junction Temperature -55 to 150 $^{\circ}$ C
Power Dissipation : Per Side^a 300 mW
Total^b 500 mW

Notes

- Derate 2.4 mW/ $^{\circ}$ C above 25 $^{\circ}$ C
- Derate 4 mW/ $^{\circ}$ C above 25 $^{\circ}$ C

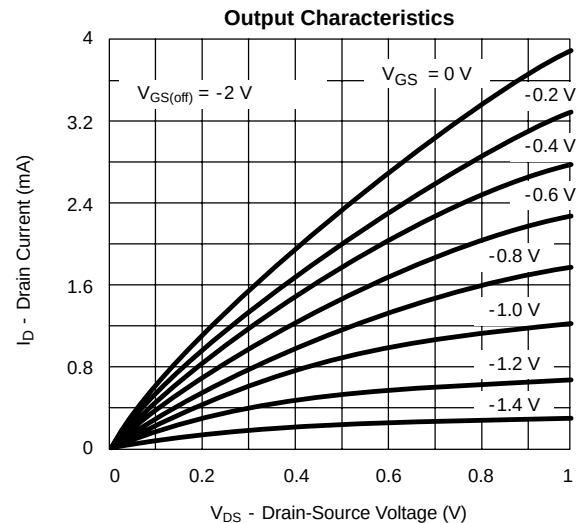
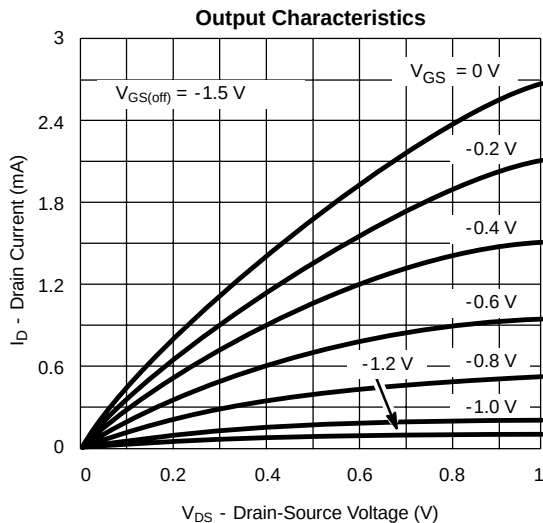
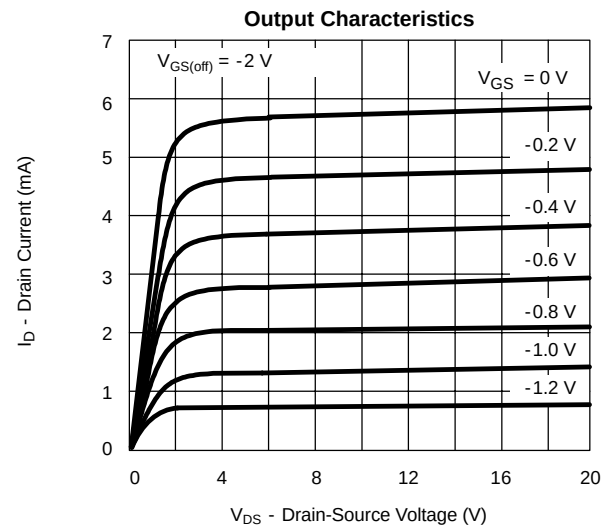
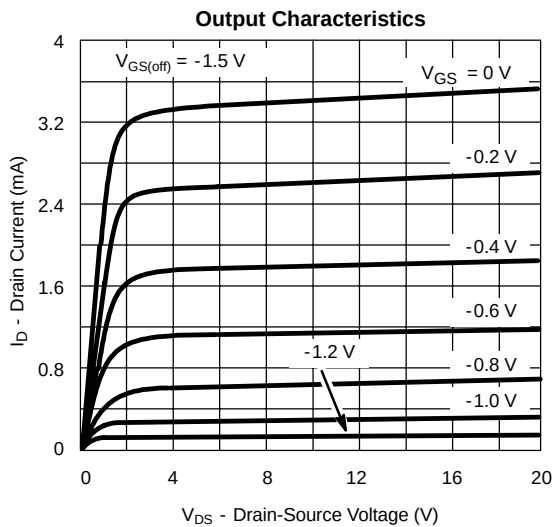
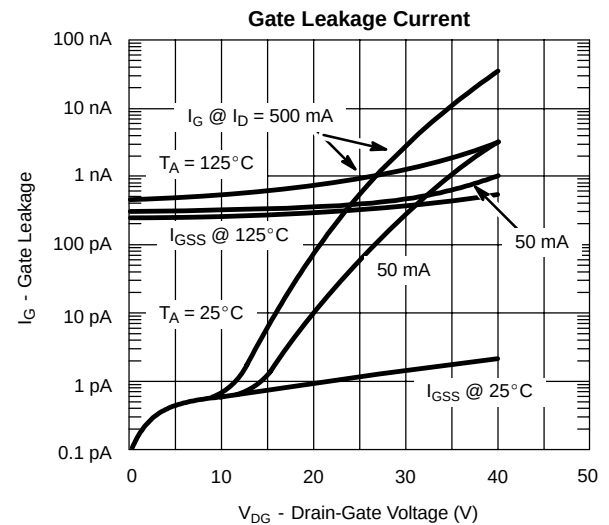
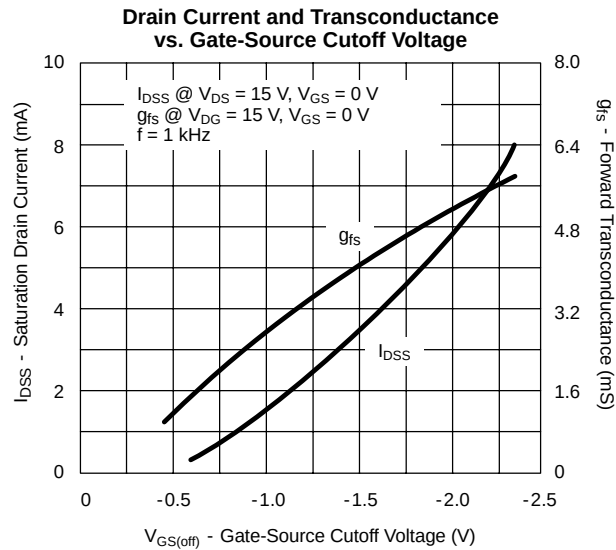


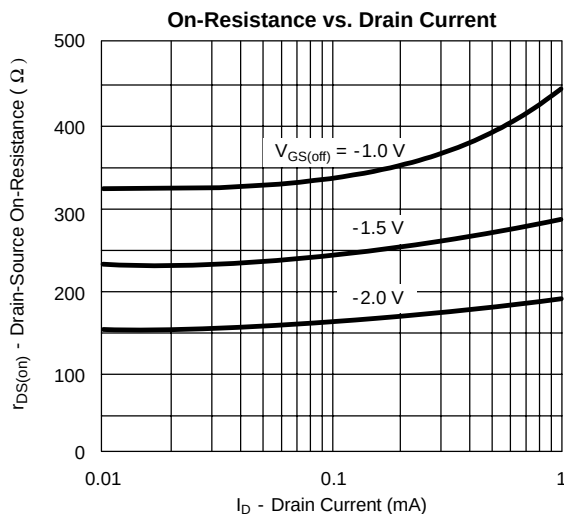
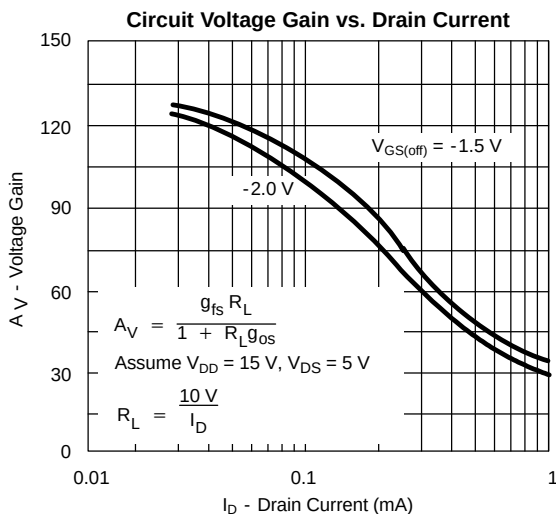
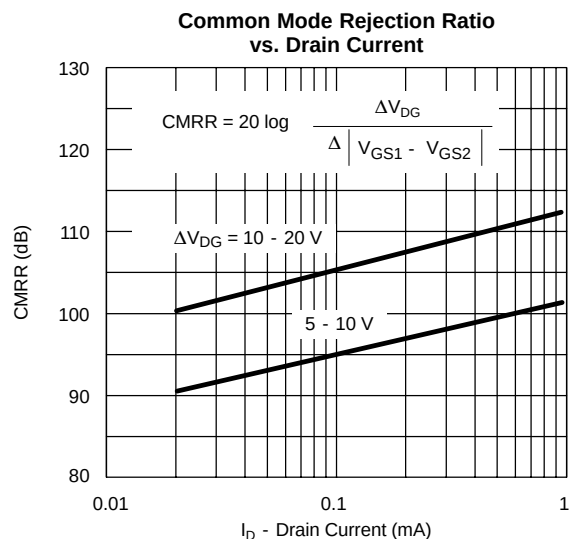
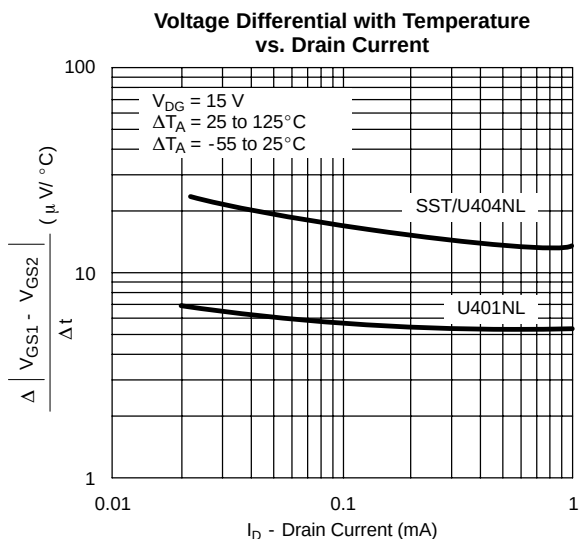
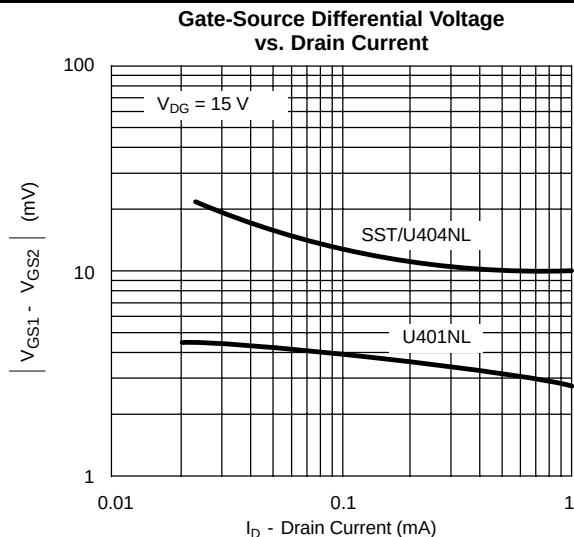
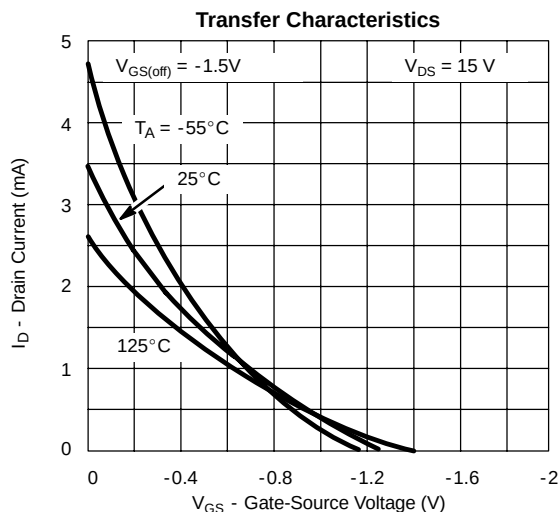
SPECIFICATIONS (T _A = 25 °C UNLESS OTHERWISE NOTED)										
Parameter	Symbol	Test Conditions	Typ ^a	Limits						Unit
				U401NL		SST/U404NL		SST/U406NL		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA, V _{DS} = 0 V	-58	-40		-40		-40		V
	V _{(BR)G1 - G2}	I _G = ±1 μA, V _{DS} = 0 V, V _{GS} = 0 V	±45	±30		±30		±30		
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 15 V, I _D = 1 nA	-1.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	
Saturation Drain Current ^b	I _{DSS}	V _{DS} = 10 V, V _{GS} = 0 V	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I _{GSS}	V _{GS} = -30 V, V _{DS} = 0 V	-2		-25		-25		-25	pA
		T _A = 125 °C	-1						nA	
Gate Operating Current	I _G	V _{DG} = 15 V, I _D = 200 μA	-2		-15		-15		-15	pA
		T _A = 125 °C	-0.8		-10		-10		-10	nA
Drain-Source On-Resistance	r _{DS(on)}	V _{GS} = 0 V, I _D = 0.1 mA	250							Ω
Gate-Source Voltage	V _{GS}	V _{DG} = 15 V, I _D = 200 μA	-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage	V _{GS(F)}	I _G = 1 mA , V _{DS} = 0 V	0.7							
Dynamic										
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 15 V, I _D = 200 μA f = 1 kHz	1.5	1	2	1	2	1	2	mS
Common-Source Output Conductance	g _{os}		1.3		2		2		2	μS
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 10 V, V _{GS} = 0 V f = 1 kHz	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g _{os}		5		30		30		30	μS
Common-Source Input Capacitance	C _{iss}	V _{DS} = 15 V, I _D = 200 μA f = 1 MHz	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C _{rss}		1.5		3		3		3	
Equivalent Input Noise Voltage	$\bar{e}_n$	V _{DS} = 15 V, I _D = 200 μA f = 10 Hz (U Only)	10		20		20		20	nV/ √Hz
Matching										
Differential Gate-Source Voltage	V _{GS1} - V _{GS2}	V _{DG} = 10 V, I _D = 200 μA			5		15		40	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	V _{DG} = 10 V I _D = 200 μA T _A = -55 to 125 °C	SST404NL	20						μV/°C
			SST406NL	40						
			All U			10		25		
Common Mode Rejection Ratio	CMRR	V _{DG} = 10 to 20 V, I _D = 200 μA	102	95		95				dB

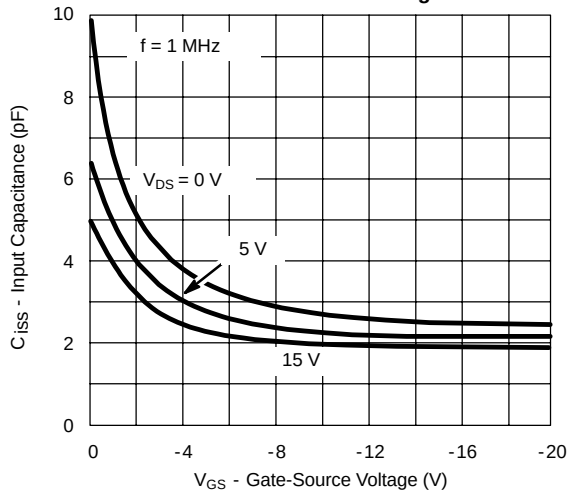
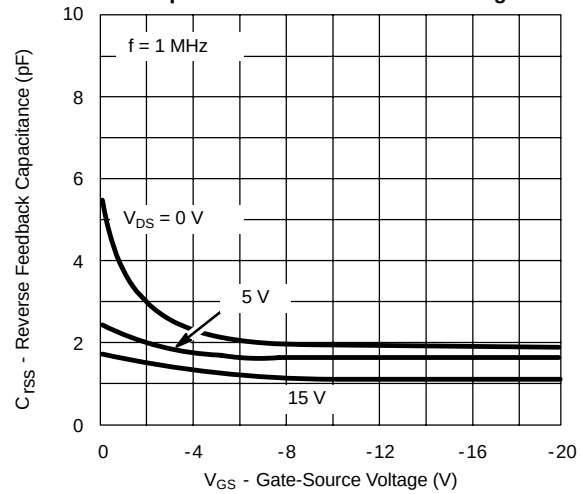
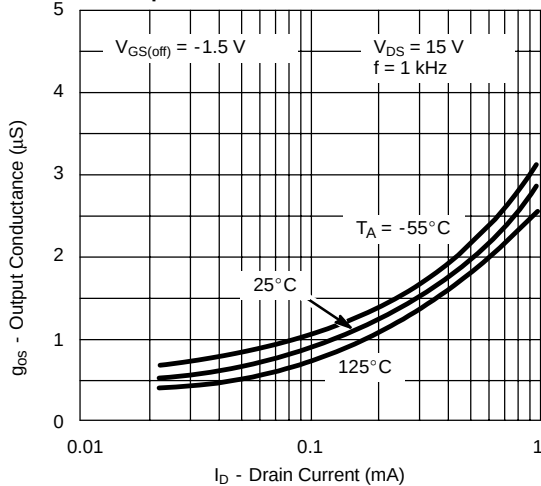
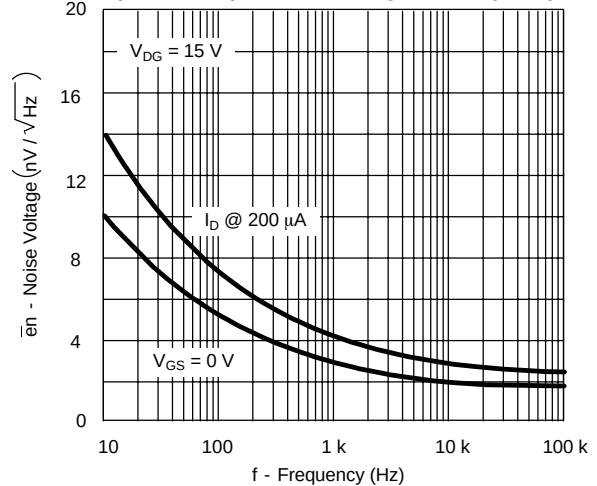
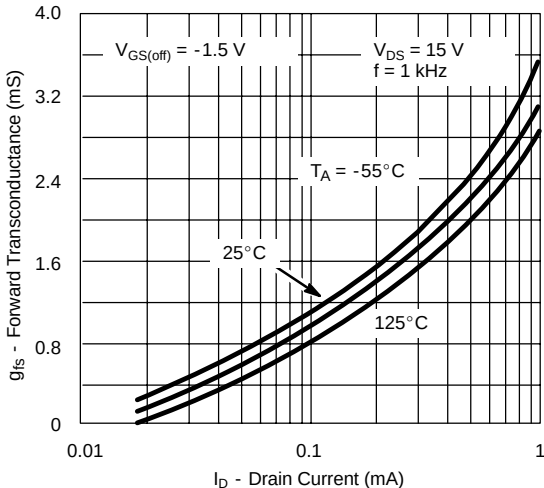
Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.

NNR

**TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)**

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)


**TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)****Common-Source Input Capacitance
vs. Gate-Source Voltage****Common-Source Reverse Feedback
Capacitance vs. Gate-Source Voltage****Output Conductance vs. Drain Current****Equivalent Input Noise Voltage vs. Frequency****Common-Source Forward Transconductance
vs. Drain Current****On-Resistance and Output Conductance
vs. Gate-Source Cutoff Voltage**