LF2242
12/16-bit Half-Band Interpolating/ Decimating Digital Filter

LOGIC DEVICES INCORPORATED

FEATURES

- 40 MHz Clock Rate
- Passband (0 to 0.22f_S) Ripple: ±0.02 dB
- Stopband (0.28f_S to 0.5f_S) Rejection: 59.4 dB
- User-Selectable 2:1 Decimation or 1:2 Interpolation
- 12-bit Two's Complement Input and 16-bit Output with User-Selectable Rounding, 8- to 16-Bits
- User-Selectable Two's Complement or Inverted Offset Binary Output Formats
- Three-State Outputs
- Replaces TRW/ Raytheon/ Fairchild TMC2242
- Package Styles Available:
  - 44-pin PLCC, J-Lead
  - 44-pin PQFP

DESCRIPTION

The **LF2242** is a linear-phase, half-band (low pass) interpolating/ decimating digital filter that, unlike intricate analog filters, requires no tuning. The LF2242 can also significantly reduce the complexity of traditional analog anti-aliasing pre-filters without compromising the signal bandwidth or attenuation. This can be achieved by using the LF2242 as a decimating post-filter with an A/D converter and by sampling the signal at twice the rate needed. Likewise, by using the LF2242 as an interpolating pre-filter with a D/A converter, the corresponding analog reconstruction post-filter circuitry can be simplified.

The coefficients of the LF2242 are fixed, and the only user programming required is the selection of the mode (interpolate, decimate, or pass-through) and rounding. The asynchronous three-state output enable control simplifies interfacing to a bus.

Data can be input into the LF2242 at a rate of up to 40 million samples per second. Within the 40 MHz I/O limit, the output sample rate can be one-half, equal to, or two times the input sample rate. Once data is clocked in, the 55-value output response begins after 7 clock cycles and ends after 61 clock cycles. The pipeline latency from the input of an impulse response to its corresponding output peak is 34 clock cycles.

The output data may be in either two's complement format or inverted offset binary format. To avoid truncation errors, the output data is always internally rounded before it is latched into the output register. Rounding is user-selectable, and the output data can be rounded from 16 bit values down to 8 bit values.

DC gain of the LF2242 is 1.0015 (0.0126 dB) in pass-through and decimate modes and 0.5007 (–3.004 dB) in interpolate mode. Passband ripple does not exceed ±0.02 dB from 0 to 0.22f_S with stopband attenuation greater than 59.4 dB from 0.28f_S to 0.5f_S (Nyquist frequency). The response of the filter is –6 dB at 0.25f_S. Full compliance with CCIR Recommendation 601 (–12 dB at 0.25f_S) can be achieved by cascading two devices serially.

LF2242 BLOCK DIAGRAM

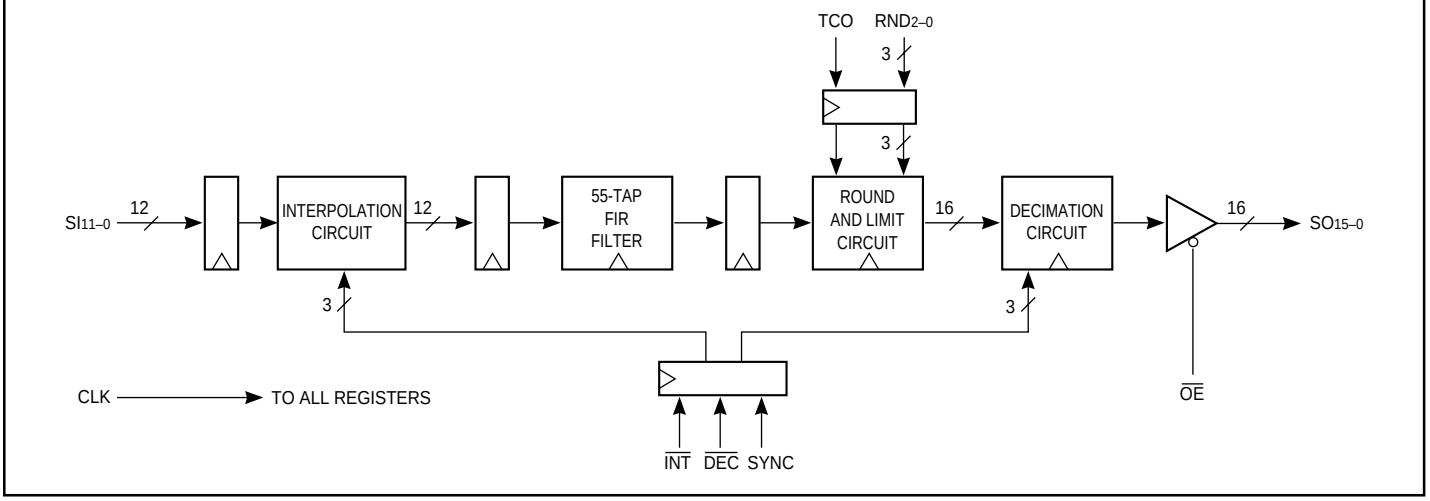
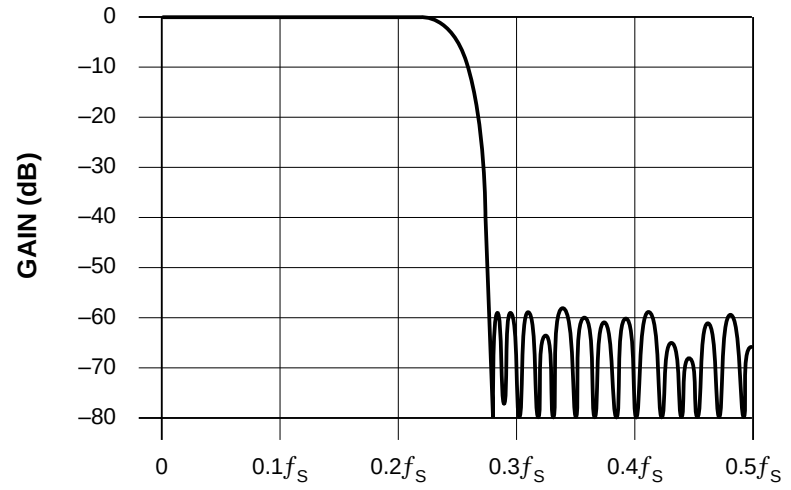


FIGURE 1. FREQUENCY RESPONSE OF FILTER



SIGNAL DEFINITIONS

Power

V_{CC} and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers. All timing specifications are referenced to the rising edge of CLK.

SYNC — Synchronization Control

Incoming data is synchronized by holding SYNC HIGH on CLK_N, and then by bringing SYNC LOW on CLK_{N+1} with the first word of input data. SYNC is held LOW until resynchronization is desired, or it can be toggled at half the clock rate. For interpolation ($\overline{INT}$ = LOW), input data should be presented at the first rising edge of CLK for which SYNC is LOW and then at every alternate rising edge of CLK thereafter. SYNC is inactive if $\overline{DEC}$ and $\overline{INT}$ are equal (pass-through mode).

Inputs

SI_{11-0} — Data Input

12-bit two's complement data input port. Data is latched into the register on the rising edge of CLK. The LSB is SI_0 (Figure 2).

Outputs

SO_{15-0} Data Output

The current 16-bit result is available on the SO_{15-0} outputs. The LF2242's limiter ensures that a valid full-scale (7FFF positive or 8000 negative) output will be generated in the event of an internal overflow. The LSB is SO_0 (Figure 2).

Controls

$\overline{INT}$ — Interpolation Control

When $\overline{INT}$ is LOW and $\overline{DEC}$ is HIGH (Table 1), the device internally forces every other incoming data sample to zero. This effectively halves the input data rate and the output amplitude.

$\overline{DEC}$ — Decimation Control

When $\overline{DEC}$ is LOW and $\overline{INT}$ is HIGH (Table 1), the output register is strobed on every other rising edge of CLK (driven at half the clock rate), decimating the output data stream.

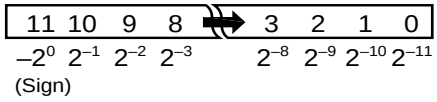
TABLE 1. MODE SELECTION

$\overline{INT}$	$\overline{DEC}$	MODE
0	0	Pass-through*
0	1	Interpolate
1	0	Decimate
1	1	Pass-through*

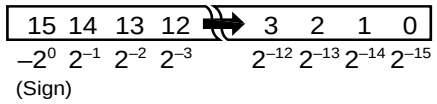
*Input and output registers run at full clock rate

FIGURE 2. INPUT AND OUTPUT FORMATS

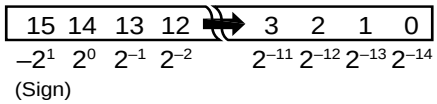
Two's Complement Input Format



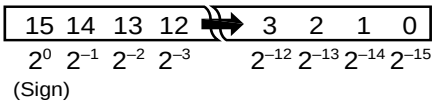
Two's Complement Output Format (TCO = 1, Non-interpolate)



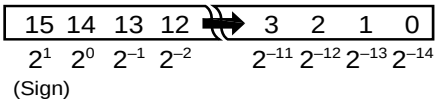
Two's Complement Output Format (TCO = 1, Interpolate)



Inverted Offset Binary Output Format (TCO = 0, Non-interpolate)



Inverted Offset Binary Output Format (TCO = 0, Interpolate)



RND2-0 — Rounding Control

The rounding control inputs set the position of the effective LSB of the output data by adding a rounding bit to the internal bit position that is one below that specified by RND2-0. All bits below the effective LSB position are subsequently zeroed (Table 2).

TCO — Two's Complement Format Control

The TCO input determines the format of the output data. When TCO is HIGH, the output data is presented in two's complement format. When TCO is LOW, the data is in inverted offset binary format (all output bits are inverted except the MSB — the MSB is unchanged).

$\overline{OE}$ — Output Enable

When the $\overline{OE}$ signal is LOW, the current data in the output register is available on the SO15-0 pins. When $\overline{OE}$ is HIGH, the outputs are in a high-impedance state.

TABLE 2. ROUNDING FORMAT

RND2-0	SO15	SO14	SO13	SO12	•••	SO8	SO7	SO6	SO5	SO4	SO3	SO2	SO1	SO0
000	X	X	X	X	•••	X	X	X	X	X	X	X	X	R
001	X	X	X	X	•••	X	X	X	X	X	X	X	R	0
010	X	X	X	X	•••	X	X	X	X	X	X	R	0	0
011	X	X	X	X	•••	X	X	X	X	X	R	0	0	0
100	X	X	X	X	•••	X	X	X	X	R	0	0	0	0
101	X	X	X	X	•••	X	X	X	R	0	0	0	0	0
110	X	X	X	X	•••	X	X	R	0	0	0	0	0	0
111	X	X	X	X	•••	X	R	0	0	0	0	0	0	0

'R' indicates the half-LSB rounded bit (effective LSB position)

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to VCC + 0.5 V
Signal applied to high impedance output ..... –0.5 V to VCC + 0.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V
Active Operation, Industrial	-40°C to +85°C	4.75 V ≤ **V**CC ≤ 5.25 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

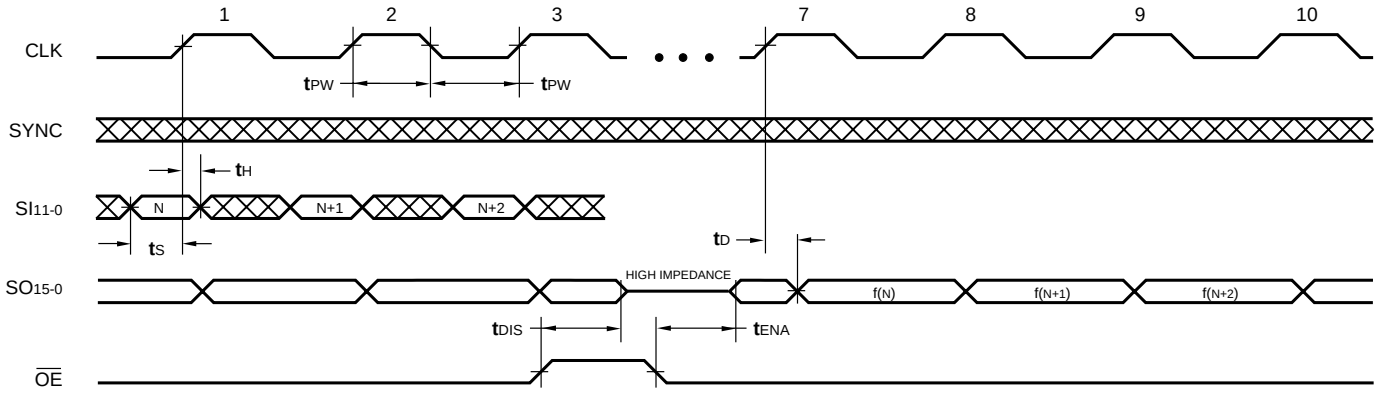
Symbol	**Parameter**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
VOH	Output High Voltage	**V**CC = Min., **I**OH = –2.0 mA	2.4			V
VOL	Output Low Voltage	**V**CC = Min., **I**OL = 4.0 mA			0.4	V
VIH	Input High Voltage		2.0		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±10	µA
IOZ	Output Leakage Current	(Note 12)			±10	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)			80	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			10	mA
CIN	Input Capacitance	**T**A = 25°C, f = 1 MHz			10	pF
COUT	Output Capacitance	**T**A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

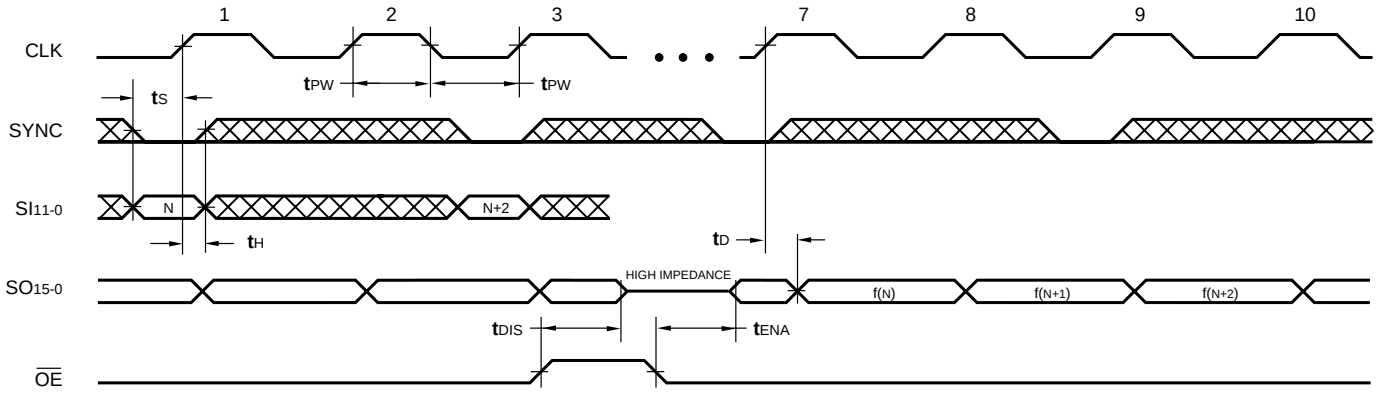
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF2242– 33 Min	LF2242– 33 Max	LF2242– 25 Min	LF2242– 25 Max
t_{CYC}	Cycle Time	33		25	
t_{PW}	Clock Pulse Width	10		10	
t_S	Input Setup Time	10		8	
t_H	Input Hold Time	0		0	
t_D	Output Delay		20		16
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15

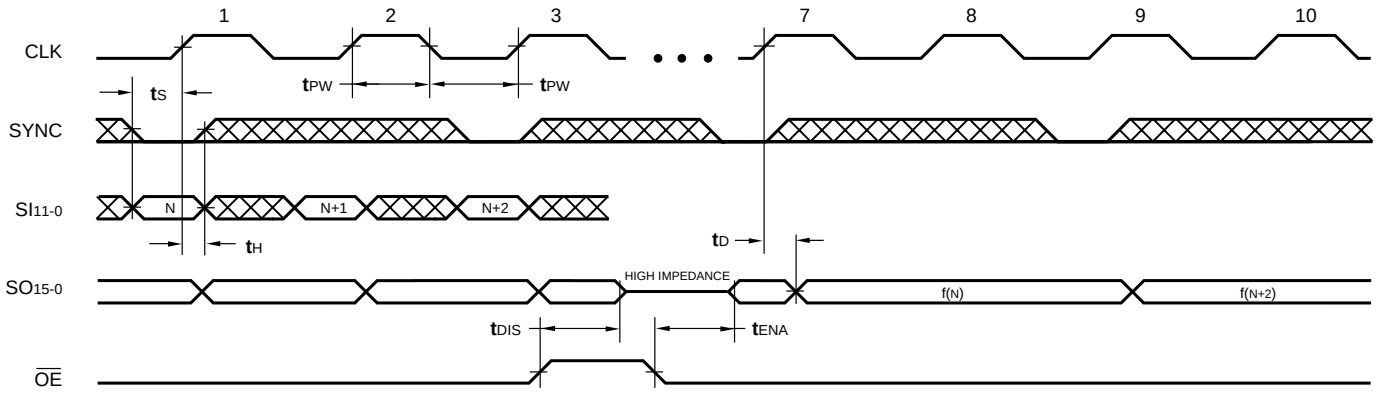
SWITCHING WAVEFORMS: PASS-THROUGH MODE ($\overline{INT}$ = $\overline{DEC}$)



SWITCHING WAVEFORMS: INTERPOLATE MODE ($\overline{INT}$ = 0, $\overline{DEC}$ = 1)



SWITCHING WAVEFORMS: DECIMATE MODE ($\overline{INT}$ = 1, $\overline{DEC}$ = 0)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

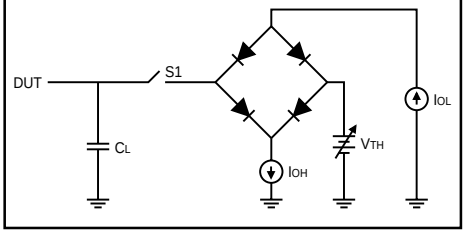
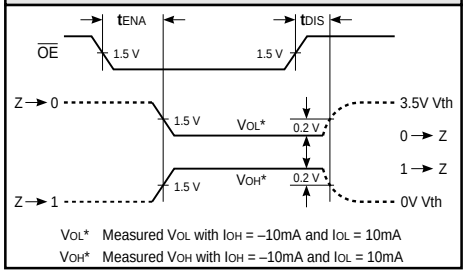
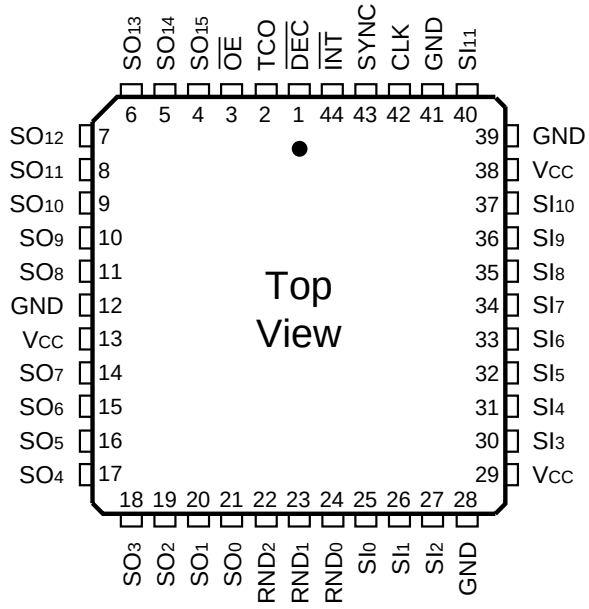


FIGURE B. THRESHOLD LEVELS

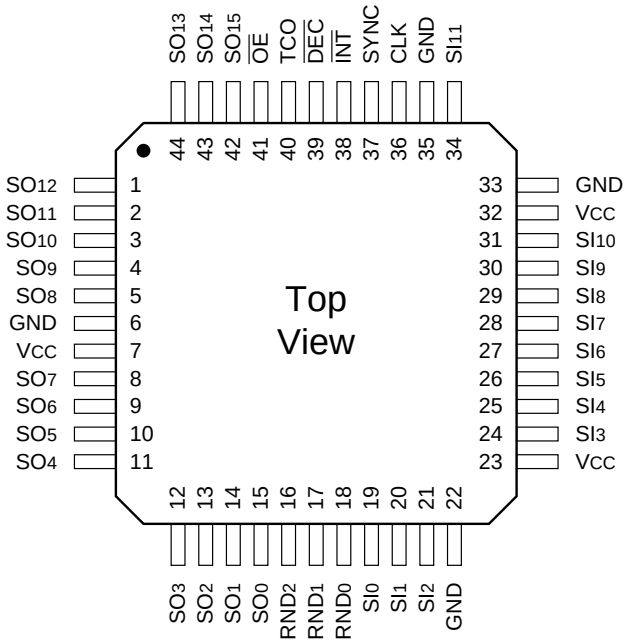


ORDERING INFORMATION

44-pin



44-pin



Speed	Plastic J-Lead Chip Carrier (J1)	Plastic Quad Flatpack (Q4)
	0°C to +70°C — COMMERCIAL SCREENING	
33 ns	LF2242JC33	LF2242QC33
25 ns	LF2242JC25	LF2242QC25
	–40°C to +85°C — COMMERCIAL SCREENING	