

Features

- 730 MHz -3 dB bandwidth (0.5 V_{PP})
- 5 ns settling to 0.2%
- V_S = ± 5 V @ 15 mA
- Low distortion: HD2, HD3 of -65 dBc at 20 MHz
- Overload/short-circuit protected
- Closed-loop, unity gain
- Low cost
- Direct replacement for CLC110

Applications

- Video buffer
- Video distribution
- HDTV buffer
- High-speed A/D buffer
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2072CN	-40°C to $+85^{\circ}\text{C}$	8-Pin P-DIP	MDP0031
EL2072CS	-40°C to $+85^{\circ}\text{C}$	8-Pin SO	MDP0027

General Description

The EL2072 is a wide bandwidth, fast settling monolithic buffer built using an advanced complementary bipolar process. This buffer is closed loop to achieve lower output impedance and higher gain accuracy. Designed for closed-loop unity gain, the EL2072 has a 730 MHz -3 dB bandwidth and 5 ns settling to 0.2% while consuming only 15 mA of supply current.

The EL2072 is an obvious high-performance solution for video distribution and line-driving applications. With low 15 mA supply current and a 70 mA output drive, performance in these areas is assured.

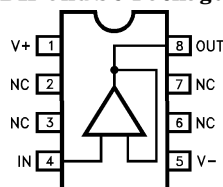
The EL2072's settling to 0.2% in 5 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 730 MHz bandwidth and extremely linear phase allow unmatched signal fidelity.

The EL2072 can be used inside an amplifier loop or PLL as its wide bandwidth and fast rise time have minimal effect on loop dynamics.

Elantec products and facilities comply with MIL-I-45028A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document *QRA-1: Elantec's Processing, Monolithic Integrated Circuits*.

Connection Diagram

DIP and SO Package



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Top View

Manufactured under U.S. Patent No. 4,893,091

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Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage (V_S)	$\pm 7\text{V}$	Operating Temperature	-40°C to $+85^\circ\text{C}$
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.	Junction Temperature	175°C
		Storage Temperature	-60°C to $+150^\circ\text{C}$
		Thermal Resistance	$\theta_{JA} = 95^\circ\text{C/W}$ P-DIP $\theta_{JA} = 175^\circ\text{C/W}$ SO
Input Voltage	$\pm V_S$	Note: See EL2071/EL2171 for Thermal Impedance curves.	

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25^\circ\text{C}$ and QA sample tested at $T_A = 25^\circ\text{C}$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25^\circ\text{C}$ for information purposes only.

DC Electrical Characteristics

$V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $R_S = 50\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Output Offset Voltage		25°C		2.0	8.0	I	mV
			T_{MIN}			16.0	V	mV
			T_{MAX}			13.0	V	mV
TCV_{OS}	Average Offset Voltage Drift		$25^\circ\text{C} - T_{MAX}$		20.0	50.0	IV	$\mu\text{V}/^\circ\text{C}$
			$25^\circ\text{C} - T_{MIN}$		20.0	100.0		
I_B	Input Bias Current		25°C , T_{MAX}		10.0	50.0	II	μA
			T_{MIN}			100.0	V	μA
TCI_B	Average Input Bias Current Drift		$25^\circ\text{C} - T_{MAX}$		200.0	300.0	IV	$\text{nA}/^\circ\text{C}$
			$25^\circ\text{C} - T_{MIN}$		200.0	700.0		
A_V	Small Signal Gain	$R_L = 100\Omega$	25°C	0.96	0.98		I	V/V
			T_{MIN} , T_{MAX}	0.95			V	V/V
ILIN	Integral End Point linearity	$\pm 2\text{V F.S.}$	25°C		0.2	0.4	IV	%F.S.
			T_{MIN}			0.8	IV	%F.S.
			T_{MAX}			0.3	IV	%F.S.
PSRR	Power Supply Rejection Ratio		All	45.0	65.0		II	dB
I_S	Supply Current—Quiescent	No Load	All		15.0	20.0	II	mA

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DC Electrical Characteristics

$V_S = \pm 5V$, $R_L = 100\Omega$, $R_S = 50\Omega$ unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
R_{IN}	Input Resistance		25°C	100.0	160.0		I	k Ω
			T_{MIN}	50.0			V	k Ω
			T_{MAX}	200.0			V	k Ω
C_{IN}	Input Capacitance		25°C		1.6	2.2	IV	pF
			T_{MIN}, T_{MAX}			2.5	IV	pF
R_{OUT}	Output Impedance (DC)		25°C		2.0	3.0	IV	Ω
			T_{MIN}, T_{MAX}			3.5	IV	Ω
I_{OUT}	Output Current		25°C, T_{MAX}	50.0	70.0		II	mA
			T_{MIN}	45.0			V	mA
V_{OUT}	Output Voltage Swing	$R_L = 100\Omega$	25°C, T_{MAX}	± 3.2	± 4.0		II	V
			T_{MIN}	± 3.0			V	V

AC Electrical Characteristics $V_S = \pm 5V$, $R_L = 100\Omega$, $R_S = 50\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
FREQUENCY RESPONSE								
SSBW	−3 dB Bandwidth (V _{OUT} < 0.5 V _{PP})		25°C	400.0	730.0		V	MHz
			T _{MIN}	400.0			IV	MHz
			T _{MAX}	300.0			IV	MHz
LSBW	−3 dB Bandwidth (V _{OUT} = 5.0 V _{PP})		25°C	55.0	90.0		IV	MHz
			T _{MIN} , T _{MAX}	50.0			IV	MHz
GAIN FLATNESS								
GFPL	Peaking V _{OUT} < 0.5 V _{PP}	< 200 MHz	25°C		0.0	0.5	V	dB
			T _{MAX}			0.6	IV	dB
			T _{MIN}			0.8	IV	dB
GFR	Rolloff V _{OUT} < 0.5 V _{PP}	< 200 MHz	25°C		0.0	0.8	V	dB
			T _{MIN}			1.0	IV	dB
			T _{MAX}			1.2	IV	dB
GDL	Group Delay	< 200 MHz	25°C, T _{MIN}		0.75	1.0	IV	ns
			T _{MAX}			1.2	IV	ns
LPD	Linear Phase Deviation V _{OUT} < 0.5 V _{PP}	< 200 MHz	25°C, T _{MIN}		0.7	1.5	IV	°
			T _{MAX}			2.0	IV	°

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AC Electrical Characteristics — Contd.

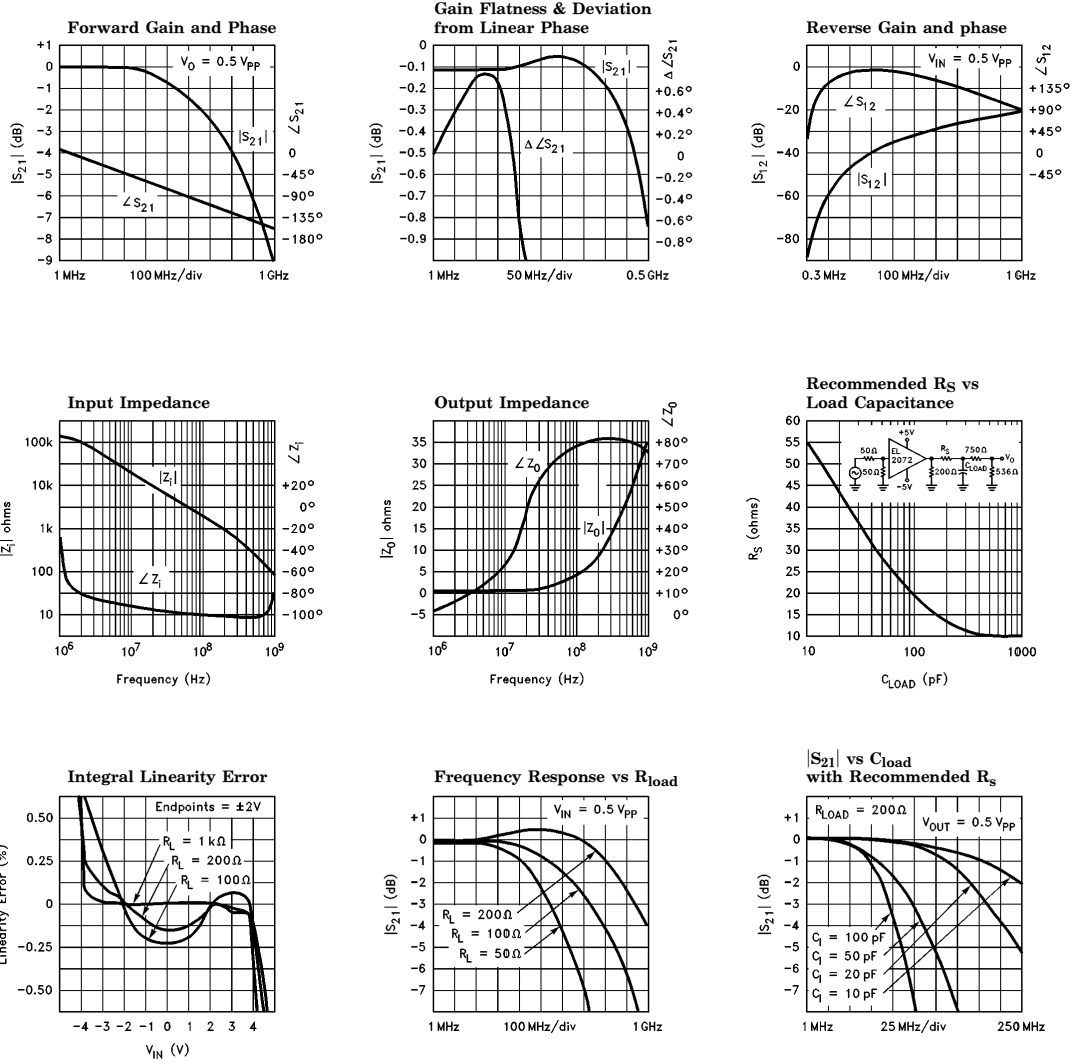
$V_S = \pm 5V$, $R_L = 100\Omega$, $R_S = 50\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
TIME-DOMAIN RESPONSE								
TR1, TF1	Rise Time, Fall Time Input Signal Rise/Fall = 300 ps	0.5V Step	25°C, T _{MIN}		0.4	1.0	IV	ns
			T _{MAX}			1.4	IV	ns
TR2, TF2	Rise Time, Fall Time Input Signal Rise/Fall ≤ 1 ns	5.0V Step	25°C		4.5	7.5	IV	ns
			T _{MIN} , T _{MAX}			8.5	IV	ns
TS1	Settling Time to 0.2% Input Signal Rise/Fall ≤ 1 ns	2.0V Step	All		5.0	10.0	IV	ns
OS	Overshoot Input Signal Rise/Fall = 300 ps	0.5V Step	25°C		0.0	10.0	IV	%
			T _{MIN} , T _{MAX}			15.0	IV	%
SR	Slew Rate		25°C	500.0	800.0		IV	V/μs
			T _{MIN} , T _{MAX}	450.0			IV	V/μs
DISTORTION								
HD2	2nd Harmonic Distortion at 20 MHz	2 V _{PP}	25°C		−55.0	−50.0	V	dBc
			T _{MIN}			−48.0	IV	dBc
			T _{MAX}			−55.0	IV	dBc
HD2A	2nd Harmonic Distortion at 50 MHz	2 V _{PP}	25°C, T _{MAX}		−50.0	−45.0	IV	dBc
			T _{MIN}			−40.0	IV	dBc
HD3	3rd Harmonic Distortion at 20 MHz	2 V _{PP}	25°C		−65.0	−55.0	V	dBc
			T _{MIN} , T _{MAX}			−55.0	IV	dBc
HD3A	3rd Harmonic Distortion at 50 MHz	2 V _{PP}	25°C, T _{MIN}		−60.0	−50.0	IV	dBc
			T _{MAX}			−45.0	IV	dBc
EQUIVALENT INPUT NOISE								
NF	Noise Floor > 100 kHz		25°C, T _{MIN}		−158.0	−155.0	IV	dBm (1 Hz)
			T _{MAX}			−154.0	IV	dBm (1 Hz)
INV	Integrated Noise 100 kHz to 200 MHz		25°C, T _{MIN}		40.0	57.0	IV	μV
			T _{MAX}			63.0	IV	μV

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Typical Performance Curves ($V_S = \pm 5V$, $R_L = 100\Omega$, $R_S = 50\Omega$)

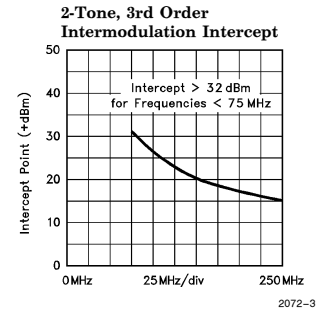
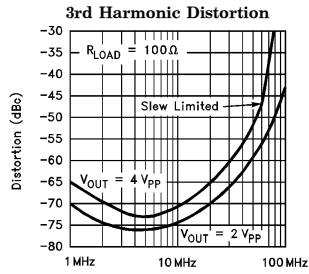
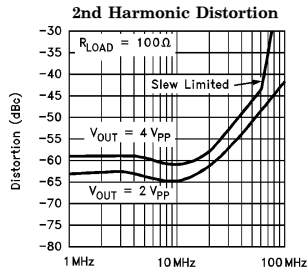
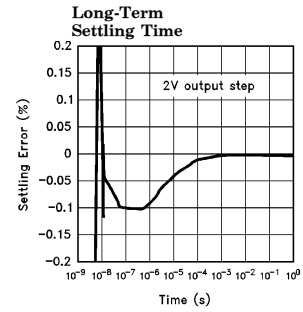
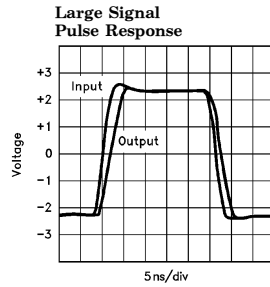
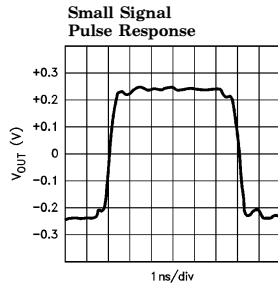


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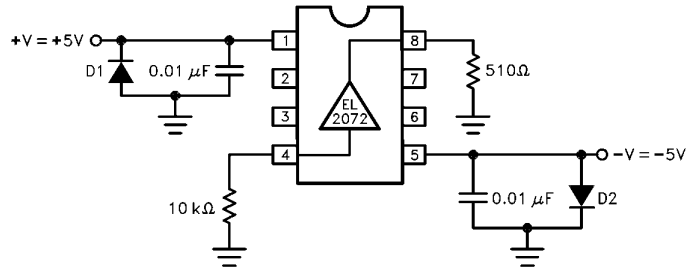
Typical Performance Curves ($V_S = \pm 5V$, $R_L = 100\Omega$, $R_S = 50\Omega$) — Contd.



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Burn-In Circuit



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Printed Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. This is especially important for the EL2072, which has a typical bandwidth of 730 MHz. Ground plane construction is a requirement, as is good power-supply bypassing close to the package. A closely-placed 0.01 μF ceramic capacitor between each supply pin and the ground plane is usually sufficient decoupling.

Pins 2, 3, 6, and 7 should be connected to the ground-plane to minimize capacitive feed-through, and all input and output traces should be laid out as transmission lines and terminated as close to the EL2072 package as possible.

Increasing capacitance on the output of the EL2072 will add phase shift, decreasing phase margin and increasing frequency-response peaking. A small series resistor before the capacitance decouples this effect, and should be used for large capacitance values. Please refer to the graphs for the appropriate resistor value to be used.

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General Disclaimer

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Elantec, Inc.

1996 Tarob Court

Milpitas, CA 95035

Telephone: (408) 945-1323

(800) 333-6314

Fax: (408) 945-9305

European Office: 44-71-482-4596

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