EL2223/EL2223C

Dual, 500 MHz High Speed, Operational Amplifier

Features

- Wide gain bandwidth—500 MHz
- High slew rate—350 V/µs
- High power bandwidth (±10 V_{out}) 5.5 MHz
- Large open loop gain 83 dB
- Low power—5 mA/amplifier
- Low input offset—0.5 mV typ.
- Wide supply voltage range V_S = ±5V to ±15V
- Output short circuit protected

Applications

- High performance active filters
- Video and pulse amplifiers
- Local area networks
- Wideband amplifiers
- Replace two HA2540s

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL2223CJ	0°C to +75°C	CerDIP	MDP0010
EL2223CN	0°C to +75°C	P-DIP	MDP0031
EL2223J	−55°C to +125°C	CerDIP	MDP0010
EL2223J/883B	−55°C to +125°C	CerDIP	MDP0010
EL2223L/883B	−55°C to +125°C	LCC	MDP0007
EL2223CM	0°C to +75°C	SOL	MDP0027

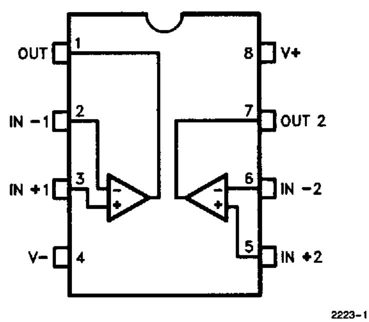
General Description

The EL2223 monolithic dual operational amplifier is an extension of Elantec's position in high speed analog products. This patented amplifier features 350 V/µs slew rate, a 500 MHz gain bandwidth gain-of-10 stable, along with an excellent speed power relationship. The dual 500 MHz EL2223 consumes only 10 mA, making it ideal for HA2540 type applications. The EL2223 has short-circuit-protected outputs and will operate from ±5V to ±15V. It is fabricated using Elantec's complementary bipolar process which allows both fast PNP and NPN transistors to be manufactured on a single chip.

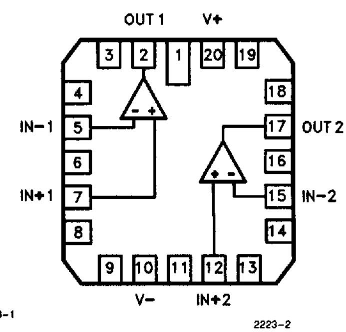
Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see Elantec document, QRA-2: *"Elantec's Military Processing, Monolithic Integrated Circuits"*.

Connection Diagrams

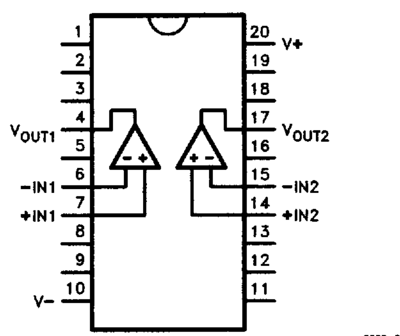
EL2223J/CN



EL2223L



EL2223CM



This product covered under U.S. Patent No. 4,837,523

EL2223/EL2223C

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Dual, 500 MHz High Speed, Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V
Differential Input Voltage	±6V
Internal Power Dissipation	See Curves
Peak Output Current	Short Circuit Protected
Output Short Circuit Duration (Note 1)	Continuous
Operational Temperature Range	
EL2223	−55°C to +125°C
EL2223C	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	
CerDIP, LCC	175°C
Plastic DIP, SOL	150°C
Lead Temperature	
DIP Package	300°C
SOL Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	Temp	EL2223 Min	EL2223 Typ	EL2223 Max	EL2223 Test Level	EL2223C Min	EL2223C Typ	EL2223C Max	EL2223C Test Level	Units
V_{OS}	Offset Voltage	+25°C Full		0.5	5 8	I I		0.5	5 8	I III	mV mV
TCV_{OS}	Average Offset Voltage Drift	Full		3		V		3		V	µV/°C
I_B	Bias Current	+25°C Full		1.5	4 6	I I		1.5	4 6	I III	µA µA
I_{OS}	Offset Current	+25°C Full		0.2	2 3	I I		0.2	2 3	I III	µA µA
R_{IN}	Input Resistance	+25°C		6		V		6		V	kΩ
C_{IN}	Input Capacitance	+25°C		1		V		1		V	pF
V_{CM}	Common Mode Input Range	Full	±10	±12		I	±10	±12		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	+25°C		7		V		7		V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (Notes 2, 3)	+25°C Full	20k 10k	40k		I I	20k 10k	40k		I III	V/V V/V

EL2223/EL2223C

Dual, 500 MHz High Speed, Operational Amplifier

DC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2\ k\Omega$, unless otherwise specified — Contd.

Parameter	Description	Temp	EL2223				EL2223C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
CMRR	Common-Mode Rejection Ratio (Note 4)	Full	70	90		I	70	90		II	dB
V_O	Output Voltage Swing	Full	±11	±12.5		I	±11	±12.5		II	V
I_{SC}	Short Circuit Current	+25°C		±50	±70	I		±50	±70	I	mA
R_O	Output Resistance	+25°C		40		V		40		V	Ω
I_s	Supply Current	Full		9.5	13	I		9.5	13	II	mA
PSRR	Power Supply Rejection Ratio (Note 5)	Full	70	90		I	70	90		II	dB

AC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2\ k\Omega$, unless otherwise specified

Parameter	Description	Temp	EL2223				EL2223C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)	+25°C		500		V		500		V	MHz
FPBW	Full Power Bandwidth (Notes 2, 7)	+25°C	3.98	5.5		I	3.98	5.5		I	MHz
t_r	Rise Time (Note 8)	+25°C		7		V		7		V	ns
OS	Overshoot (Note 8)	+25°C		30		V		30		V	%
SR	Slew Rate (Note 8)	+25°C	250	350		I	250	350		I	V/μs
t_s	Settling Time (Notes 9, 10) 10V Step to 0.05%	+25°C		330		V		330		V	ns
Ch S_p	Channel Separation (f = 10 MHz)			70		V		70		V	dB

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: $V_O = \pm 10V$.
Note 3: RL = 2 kΩ.
Note 4: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 5: Two tests are performed. V+ = 15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 6: V_O = 100 mV.
Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/ $2 \pi V_{peak}$.
Note 8: Refer to Test Circuit section of data sheet.
Note 9: Settling time measurement are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN September 19, 1985.
Note 10: $A_V = +10$, $R_L = 2\ k\Omega$.

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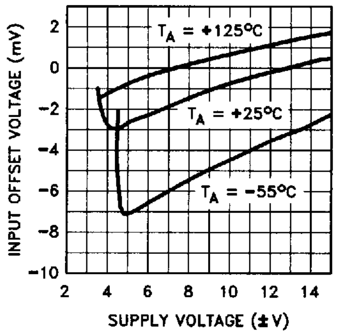
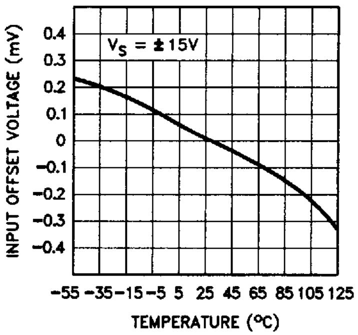
Typical Performance Curves

Input Offset Voltage vs Supply Voltage



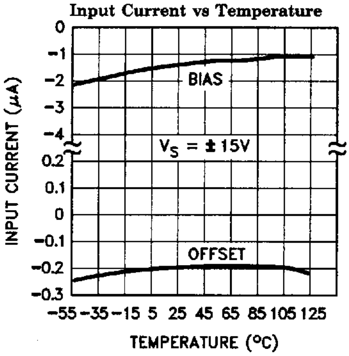
2223-4

Normalized Input Offset Voltage vs Temperature



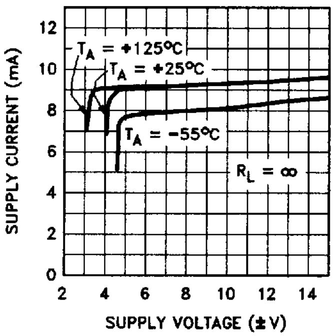
2223-5

Input Current vs Temperature



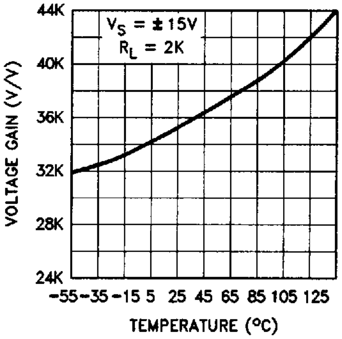
2223-6

Supply Current vs Supply Voltage



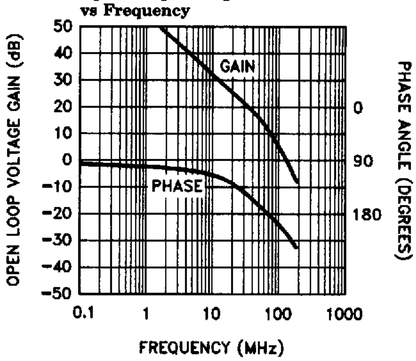
2223-7

Voltage Gain vs Temperature



2223-8

Open Loop Voltage Gain vs Frequency



2223-9

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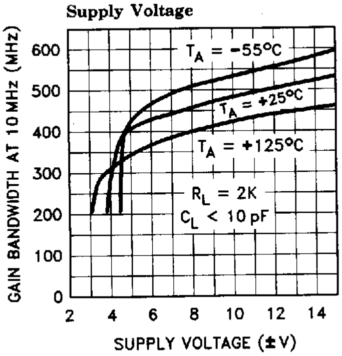
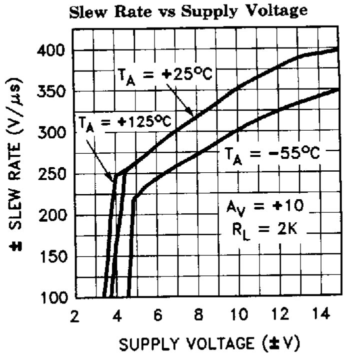
Typical Performance Curves — Contd.

Gain Bandwidth at 10 MHz vs Supply Voltage



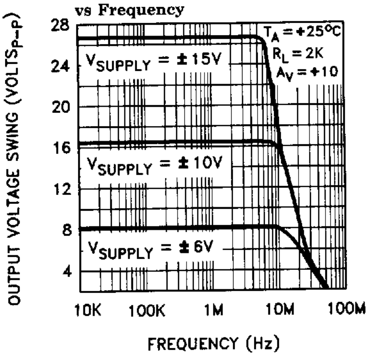
2223-10

Slew Rate vs Supply Voltage



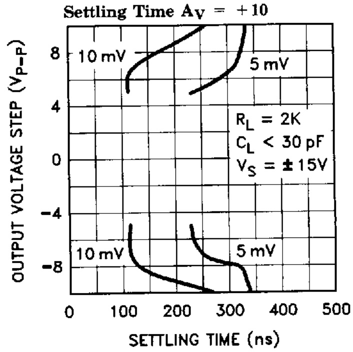
2223-11

Output Voltage Swing vs Frequency



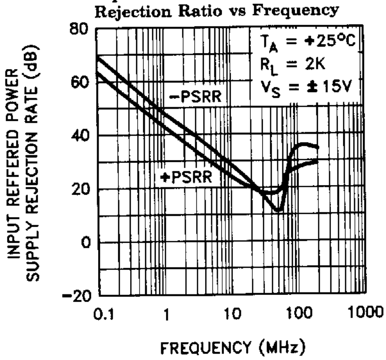
2223-12

Settling Time A_V = +10



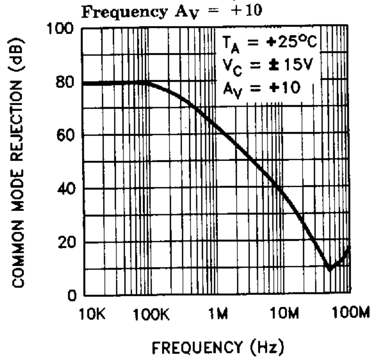
2223-13

Input Referred Power Supply Rejection Ratio vs Frequency



2223-14

Common Mode Rejection vs Frequency A_V = +10



2223-15

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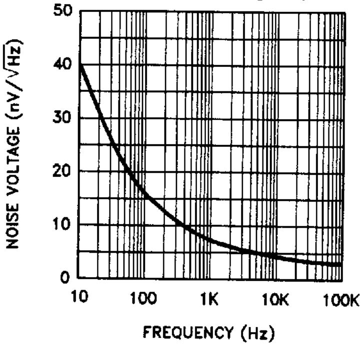
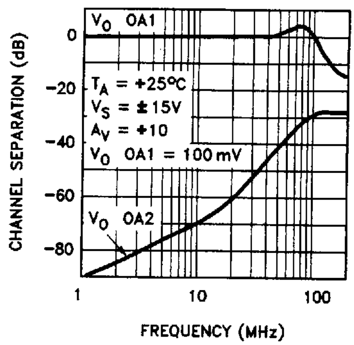
Typical Performance Curves — Contd.

Noise Voltage vs Frequency



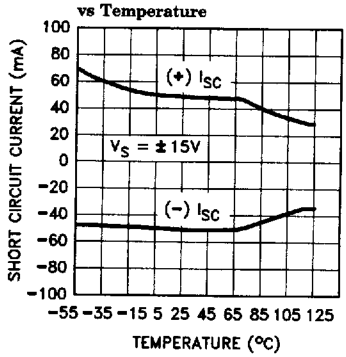
2223-16

Channel Separation vs Frequency



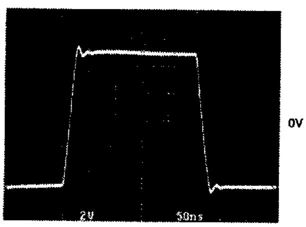
2223-17

Short Circuit Current vs Temperature



2223-18

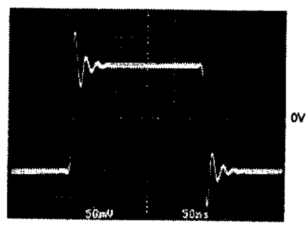
Large Signal Response



A_V = +10
V_{IN} = ±0.5V
V_O = ±5V
R_L = 2k

2223-19

Small Signal Response

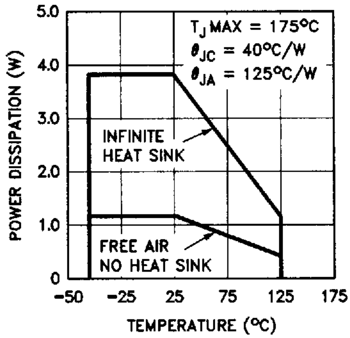


A_V = +10
V_{IN} = ±10 mV
V_O = ±100 mV
R_L = 2k

2223-20

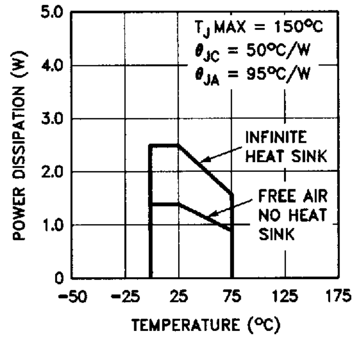
Typical Performance Curves — Contd.

8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



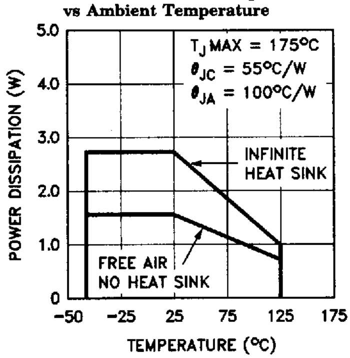
2223-21

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



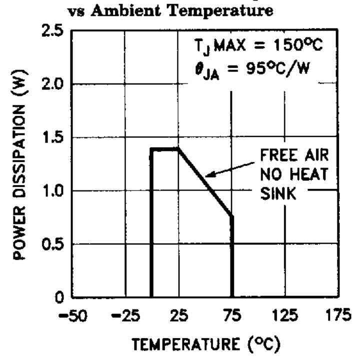
2223-22

20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



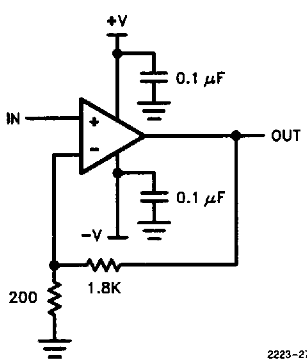
2223-23

20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2223-24

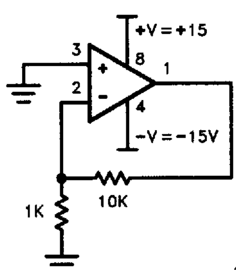
Test Circuit



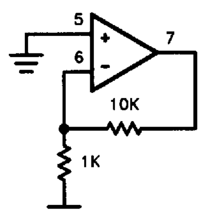
2223-27

A_V = +10
$C_L \leq$ 10 pF Scope Probe

Burn-In Circuit



2223-28



2223-29

Pin numbers are for the 8-Lead CerDIP.
Burn-in circuit is identical for all package types.

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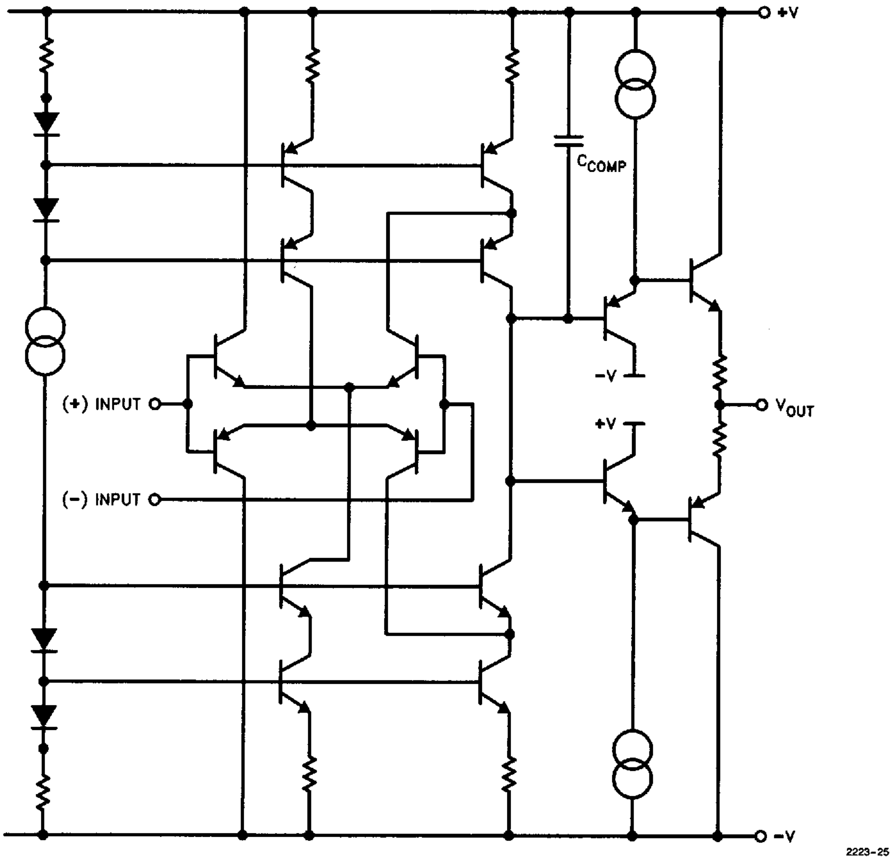
Simplified Schematic (one amplifier)



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EL2223 Macromodel

```
* Connections:  +input
*               |     -input
*               |     |     +Vsupply
*               |     |     |     -Vsupply
*               |     |     |     |     output
*               |     |     |     |     |
.subckt M2233   3     2     7     4     6
* Input stage
ie 37 4 2mA
r6 36 37 60
r7 38 37 60
rc1 7 30 75
rc2 7 39 75
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 7.25
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 2.6m
rh 34 0 3Meg
ch 34 0 1.5pF
rc 34 40 600
cc 40 0 7pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 25pF
rpb 42 43 50
cpb 43 0 15pF
* Output Stage
ios1 7 50 1.25mA
ios2 51 4 1.25mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
* models
.model qn npn (is=800.0E-18 bf=250 tf=0.2nS)
.model qna npn (is=864E-18 bf=300 tf=0.2nS)
.model qp pnp (is=800E-18 bf=60 tf=0.2nS)
.ends
```

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ELANTEC INC

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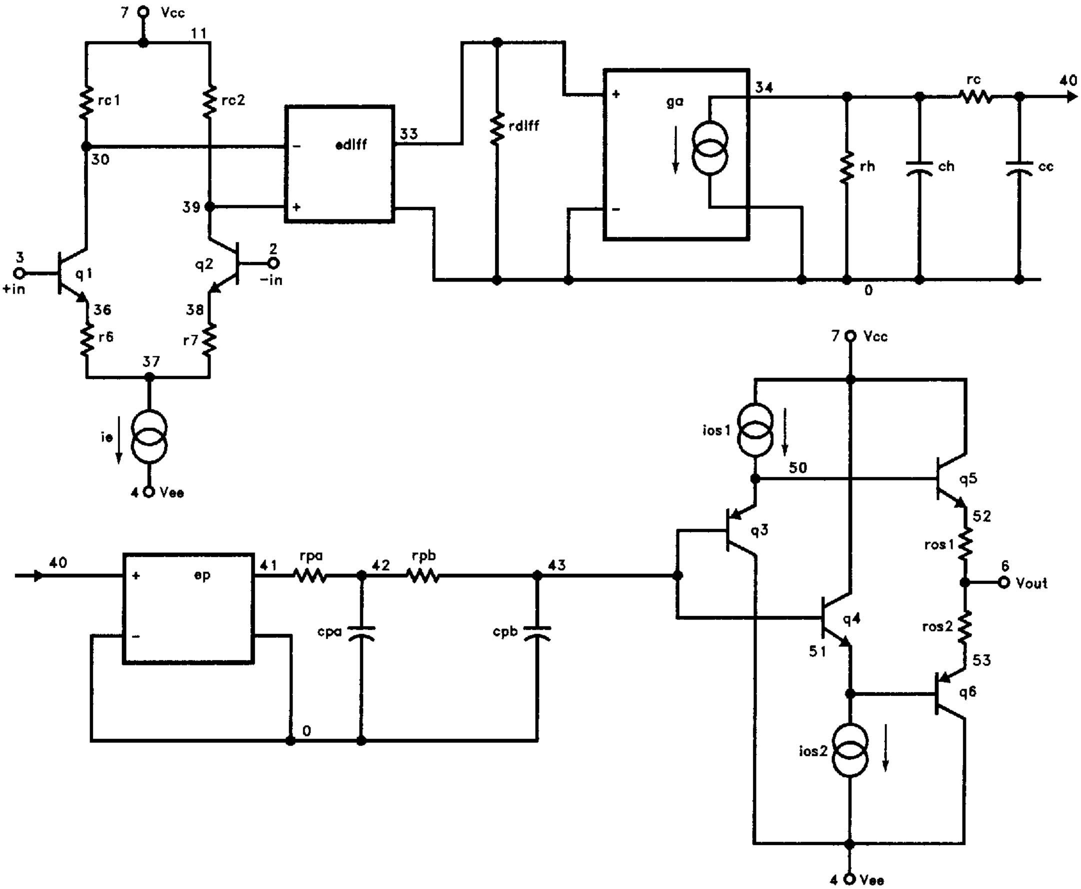
EL2223 Macromodel — Contd.



2223-30