

# P-Channel JFET Switch



## J174 – J177 / SST174 – SST177

### FEATURES

- Low Insertion Loss
- No Offset or Error Generated By Closed Switch
  - Purely Resistive
  - High Isolation Resistance From Driver
- Short Sample and Hold Aperture Time
- Fast Switching

### APPLICATIONS

- Analog Switches
- Choppers
- Commutators

### ABSOLUTE MAXIMUM RATINGS

(T<sub>A</sub> = 25°C unless otherwise specified)

Gate-Drain or Gate-Source Voltage . . . . . 30V  
Gate Current . . . . . 50mA  
Storage Temperature Range . . . . . -55°C to +150°C  
Operating Temperature Range . . . . . -55°C to +135°C  
Lead Temperature (Soldering, 10sec) . . . . . 300°C  
Power Dissipation . . . . . 350mW  
Derate above 25°C . . . . . 3.3mW/°C

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ORDERING INFORMATION

| Part          | Package        | Temperature Range |
|---------------|----------------|-------------------|
| J174-J177     | Plastic TO-92  | -55°C to +135°C   |
| SST174-SST177 | Plastic SOT-23 | -55°C to +135°C   |

For Sorted Chips in Carriers see 2N5114 series.

**PIN CONFIGURATION**

TO-92

SOT-23

**5508**

| PRODUCT MARKING (SOT-23) |     |
|--------------------------|-----|
| SST174                   | P04 |
| SST175                   | P05 |
| SST176                   | P06 |
| SST177                   | P07 |



# **ELECTRICAL CHARACTERISTICS** ( $T_A = 25^{\circ}\text{C}$ unless otherwise specified)

| SYMBOL                                    | PARAMETER                                  | J174 |     |      | J175 |     |     | J176 |     |     | J177 |     |      | UNITS | TEST CONDITIONS                                |                   |      |
|-------------------------------------------|--------------------------------------------|------|-----|------|------|-----|-----|------|-----|-----|------|-----|------|-------|------------------------------------------------|-------------------|------|
|                                           |                                            | MIN  | TYP | MAX  | MIN  | TYP | MAX | MIN  | TYP | MAX | MIN  | TYP | MAX  |       |                                                |                   |      |
| I <sub>GSS</sub>                          | Gate Reverse Current (Note 1)              |      |     | 1    |      |     | 1   |      |     | 1   |      |     | 1    | nA    | V <sub>DS</sub> = 0, V <sub>GS</sub> = 20V     |                   |      |
| V <sub>GS(off)</sub>                      | Gate Source Cutoff Voltage                 | 5    |     | 10   | 3    |     | 6   | 1    |     | 4   | 0.8  |     | 2.25 | V     | V <sub>DS</sub> = -15V, I <sub>D</sub> = -10nA |                   |      |
| BV <sub>GSS</sub>                         | Gate Source Breakdown Voltage              | 30   |     |      | 30   |     |     | 30   |     |     | 30   |     |      |       | V <sub>DS</sub> = 0, I <sub>G</sub> = 1μA      |                   |      |
| I <sub>DSS</sub>                          | Drain Saturation Current (Note 2)          | -20  |     | -135 | -7   |     | -70 | -2   |     | -35 | -1.5 |     | -20  | mA    | V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0    |                   |      |
| I <sub>D(off)</sub>                       | Drain Cutoff Current (Note 1)              |      |     | -1   |      |     | -1  |      |     | -1  |      |     | -1   | nA    | V <sub>DS</sub> = -15V, V <sub>GS</sub> = 10V  |                   |      |
| r <sub>DS(on)</sub>                       | Drain-Source ON Resistance                 |      |     | 85   |      |     | 125 |      |     | 250 |      |     | 300  | Ω     | V <sub>GS</sub> = 0, V <sub>DS</sub> = -0.1V   |                   |      |
| C <sub>dg(off)</sub>                      | Drain-Gate OFF Capacitance                 |      | 5.5 |      |      | 5.5 |     |      | 5.5 |     |      | 5.5 |      | pF    | V <sub>DS</sub> = 0, V <sub>GS</sub> = 10V     | f = 1MHz (Note 3) |      |
| C <sub>sg(off)</sub>                      | Source-Gate OFF Capacitance                |      | 5.5 |      |      | 5.5 |     |      | 5.5 |     |      | 5.5 |      |       | V <sub>DS</sub> = V <sub>GS</sub> = 0          |                   |      |
| C <sub>dg(on)</sub> + C <sub>sg(on)</sub> | Drain-Gate Plus Source Gate ON Capacitance |      | 32  |      |      | 32  |     |      | 32  |     |      | 32  |      |       |                                                |                   |      |
| t <sub>d(on)</sub>                        | Turn On Delay Time                         |      | 2   |      |      | 5   |     |      | 15  |     |      | 20  |      | ns    | Switching Time Test Conditions (Note 3)        |                   |      |
| t <sub>r</sub>                            | Rise Time                                  |      | 5   |      |      | 10  |     |      | 20  |     |      | 25  |      |       | V <sub>DD</sub>                                | J174              | J175 |
| t <sub>d(off)</sub>                       | Turn Off Delay Time                        |      | 5   |      |      | 10  |     |      | 15  |     |      | 20  |      |       | V <sub>GS(off)</sub>                           | 12V               | 8V   |
| t <sub>f</sub>                            | Fall Time                                  |      | 10  |      |      | 20  |     |      | 20  |     |      | 25  |      |       | R <sub>L</sub>                                 | 560Ω              | 12kΩ |

- NOTES:**
1. Approximately doubles for every  $10^{\circ}\text{C}$  increase in  $T_A$ .
  2. Pulse test duration  $\sim 300\mu s$ ; duty cycle  $\leq 3\%$ .
  3. For design reference only, not 100% tested.