

N-Channel JFET Monolithic Dual



SST5912

FEATURES

- High Gain $g_{fs} > 6 \text{ mS}$
- Low Leakage $I_G < 1 \text{ pA typical}$
- Low Noise
- Surface Mount Package

APPLICATIONS

- Differential Wideband Amplifier
- VHF/UHF Amplifiers
- Test and Measurement

DESCRIPTION

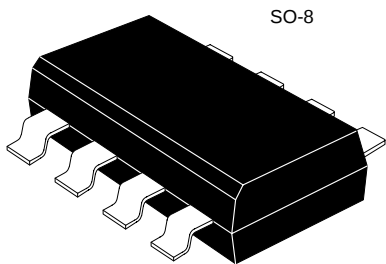
The SST5912 is a High Speed N-Channel Monolithic JFET pair encapsulated in a surface mount plastic SO-8 package. The device is designed for high gain (typically $> 6000 \text{ mmhos}$), low leakage ($< 1 \text{ pA typical}$) and low noise. The SST5912 is an excellent choice for differential wideband amplifiers, VHF/UHF amplifiers and test and measurement.

ORDERING INFORMATION

Part	Package	Temperature Range
SST5912	Plastic SO-8 Package	-55°C to $+150^{\circ}\text{C}$

NOTE: For Sorted Chips in Carriers, See 2N5911 Series

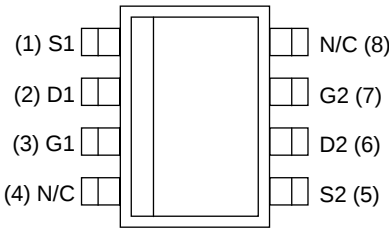
PIN CONFIGURATION



SO-8

CJ1

TOP VIEW



PRODUCT MARKING

PRODUCT MARKING	
SST5912	SST5912

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter/Test Condition	Symbol	Limit	Unit
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	V
Forward Gate Current	I_G	50	mA
Power Dissipation (per side)	P_D	300	mW
(total)		500	mW
Power Derating (per side)		2.4	mW/ $^{\circ}\text{C}$
(total)		4	mW/ $^{\circ}\text{C}$
Operating Junction Temperature	T_J	-55 to 150	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-65 to 150	$^{\circ}\text{C}$
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

SYMBOL	CHARACTERISTICS	TYP ¹	SST5912		UNIT	TEST CONDITIONS	
			MIN	MAX			
STATIC							
V _{(BR)GSS}	Gate-Source Breakdown Voltage	-35	-25		V	I _G = -1mA, V _{DS} = 0V	
V _{GS(OFF)}	Gate-Source Cut off Voltage	-3.5	-1	-5		V _{DS} = 10V, I _D = 1nA	
I _{DSS}	Saturation Drain Current ²	15	7	40	mA	V _{DS} = 10V, V _{GS} = 0V	
I _{GSS}	Gate Reverse Current	-1		-100	pA	V _{GS} = -15V, V _{DS} = 0V	
		-0.2			nA	T _A = 125°C	
I _G	Gate Operating Current	-1		-100	pA	V _{DG} = 10V, I _D = 5mA	
		-0.2			nA	T _A = 125°C	
V _{GS}	Gate-Source Voltage	-1.5	-0.3	-4	V	V _{DG} = 10V, I _D = 5mA	
V _{GS(F)}	Gate-Source Forward Voltage	0.7				I _G = 1mA, V _{DS} = 0V	
DYNAMIC							
g _{fs}	Common-Source Forward Transconductance	6	5	10	mS	V _{DG} = 10V, I _D = 5mA	
g _{os}	Common-Source Output Conductance	20		100	mS	f = 1kHz	
g _{fs}	Common-Source Forward Transconductance	6	5	10	mS	V _{DG} = 10V, I _D = 5mA	
g _{os}	Common-Source Output Conductance	30		150	mS	f = 100MHz	
C _{iss}	Common-Source Input Capacitance	3.5		5	pF	V _{DG} = 10V, I _D = 5mA	
C _{rss}	Common-Source Reverse Transfer Capacitance	1		1.2		f = 1MHz	
$\bar{e}_n$	Equivalent Input Noise Voltage	4		20	nV/ $\sqrt{\text{Hz}}$	V _{DG} = 10V, I _D = 5mA, f = 10kHz	
NF	Noise Figure	0.1		1	dB	V _{DG} = 10V, I _D = 5mA, f = 10kHz, R _G = 100W	
MATCHING							
V _{GS1} - V _{GS2}	Differential Gate Source Voltage	7		15	mV	V _{DG} = 10V, I _D = 5mA	
$\frac{D V_{GS1} - V_{GS2} }{DT}$	Gate Source Voltage Differential Change with Temperature	10		40	mV/°C	T = -55 to 25°C	
		10		40		T = 25 to 125°C	
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.98	0.95	1		V _{DS} = 10V, V _{GS} = 0V	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.98	0.95	1		V _{DG} = 10V, I _D = 5mA, f = 1kHz	
I _{G1} - I _{G2}	Differential Gate Current	0.01		20	nA	V _{DG} = 10V, I _D = 5mA, T _A = 125°C	
CMRR	Common Mode Rejection Ratio	90			dB	V _{DD} = 5 to 10V, I _D = 5mA	

NOTES: 1. For design aid only, not subject to production testing.
2. Pulse test; PW = 300ms, duty cycle $\hat{a}$ 3%.