To all our customers

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Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SJ484

Silicon P-Channel MOS FET
High Speed Power Switching

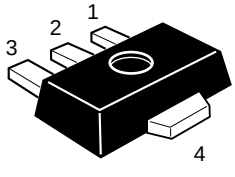
ADE-208-501A (Z)
2nd. Edition
Mar. 2001

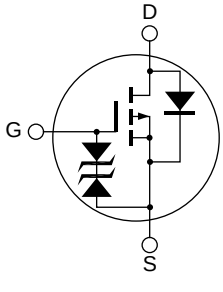
Features

- Low on-resistance
  $R_{DS(on)}$ = 0.18 Ω typ. (at V_{GS} = –10V, I_D = –1A)
- Low drive current
- High speed switching
- 4V gate drive devices.

Outline

UPAK





1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–2	A
Drain peak current	$I_{D(pulse)}$*[1]	–4	A
Body to drain diode reverse drain current	I_{DR}	–2	A
Channel dissipation	Pch*[2]	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 100µs, duty cycle ≤ 10 %
2. When using aluminium ceramic board (12.5 x 20 x 0.7 mm)

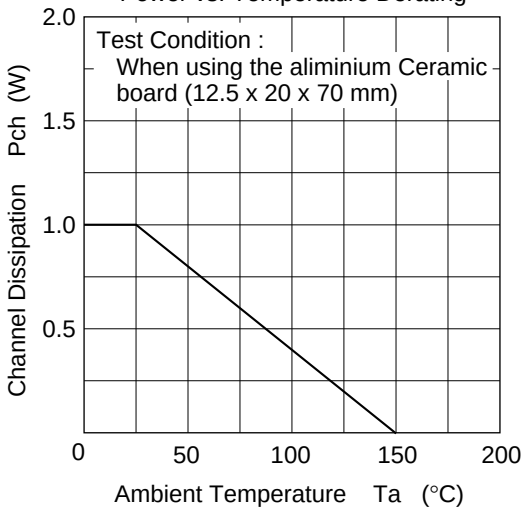
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1mA, V_{DS} = –10V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.18	0.23	Ω	I_D = –1A, V_{GS} = –10V*[1]
	$R_{DS(on)}$	—	0.3	0.45	Ω	I_D = –1A, V_{GS} = –4V*[1]
Forward transfer admittance	$\|y_{fs}\|$	1.2	2.0	—	S	I_D = –1A, V_{DS} = –10V*[1]
Input capacitance	Ciss	—	230	—	pF	V_{DS} = –10V
Output capacitance	Coss	—	140	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	50	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	I_D = –1A, R_L = 30Ω
Rise time	t_r	—	30	—	ns	V_{GS} = –10V
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	30	—	ns	
Body to drain diode forward voltage	V_{DF}	—	–0.95	—	V	I_F = –2A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	60	—	ns	I_F = –2A, V_{GS} = 0 diF/ dt = 50A/µs

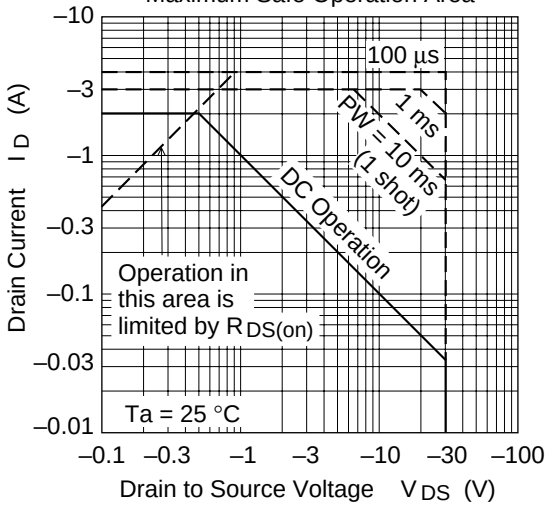
Notes: 1. Pulse test
2. Marking is “WY”.

Main Characteristics

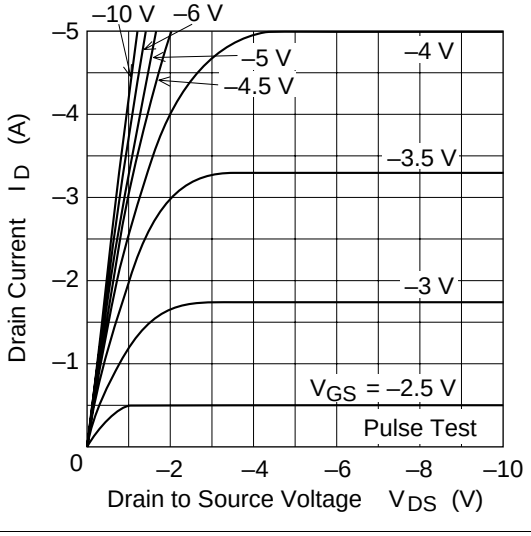
Power vs. Temperature Derating



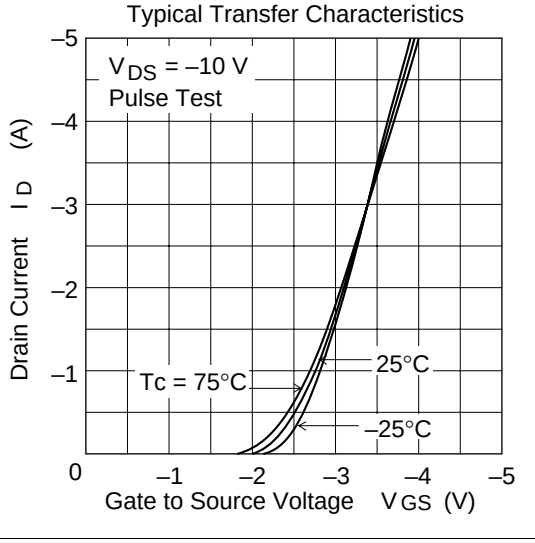
Maximum Safe Operation Area



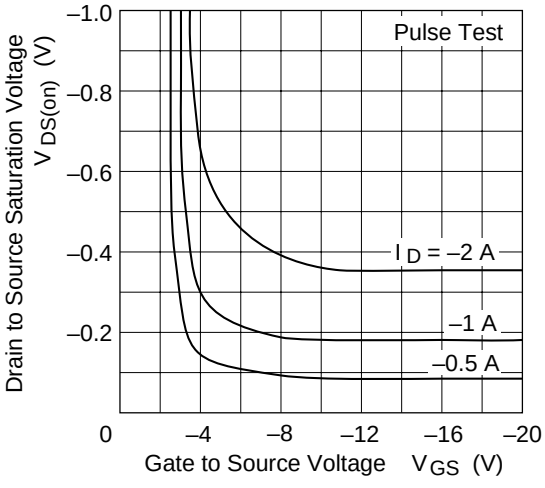
Typical Output Characteristics



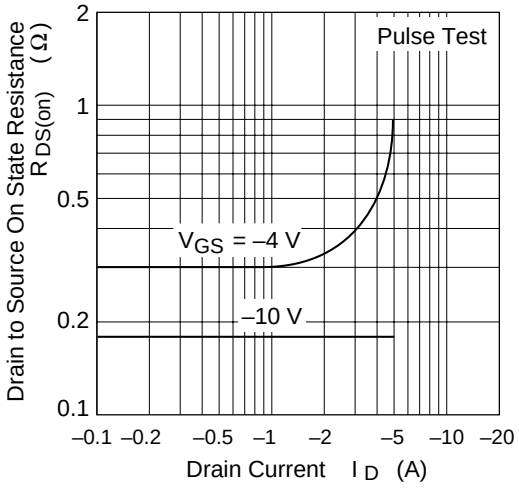
Typical Transfer Characteristics



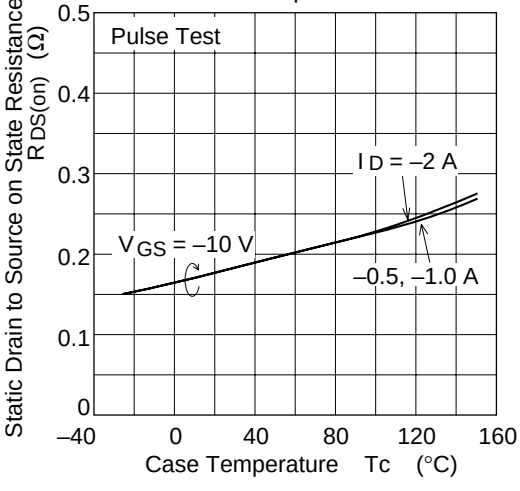
Drain to Source Saturation Voltage vs. Gate to Source Voltage



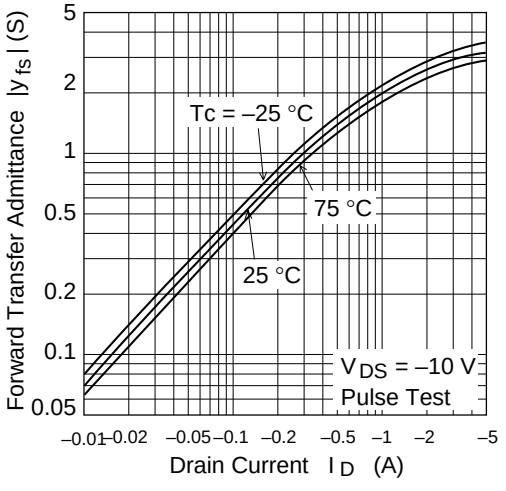
Static Drain to Source on State Resistance vs. Drain Current



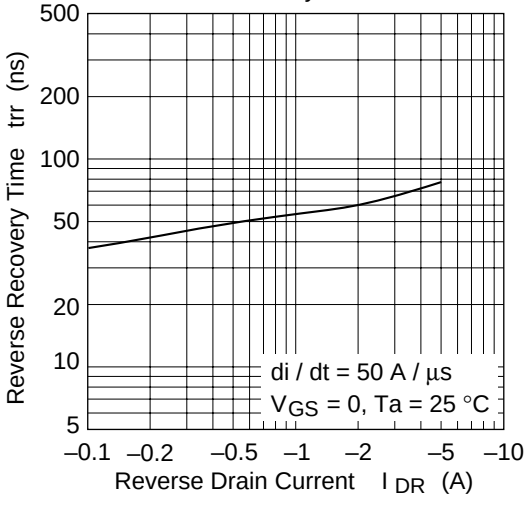
Static Drain to Source on State Resistance vs. Temperature



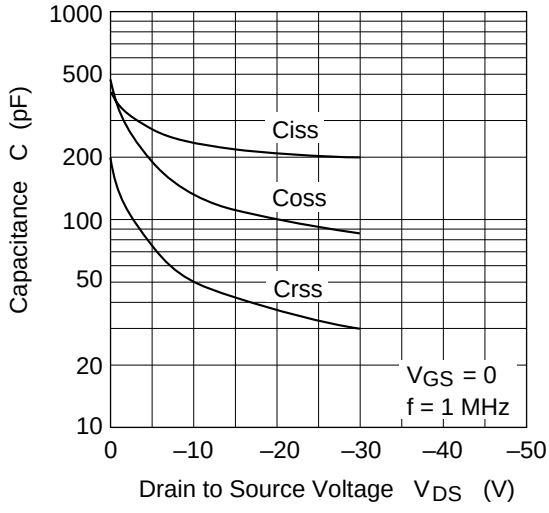
Forward Transfer Admittance vs. Drain Current



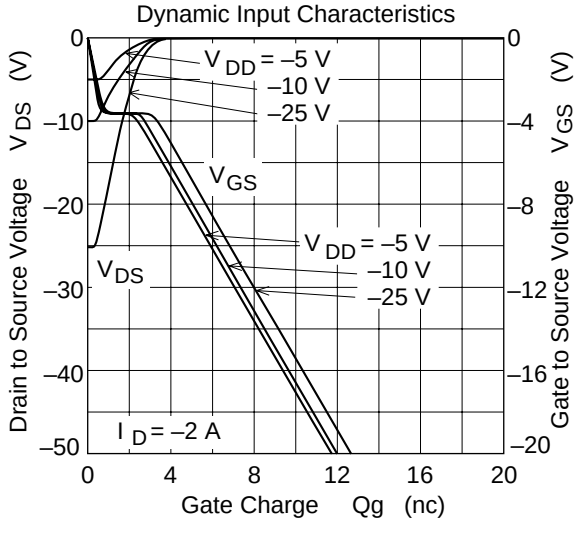
Body to Drain Diode Reverse Recovery Time



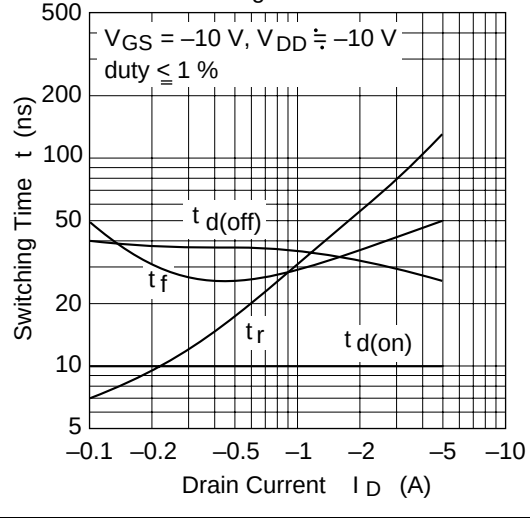
Typical Capacitance vs. Drain to Source Voltage



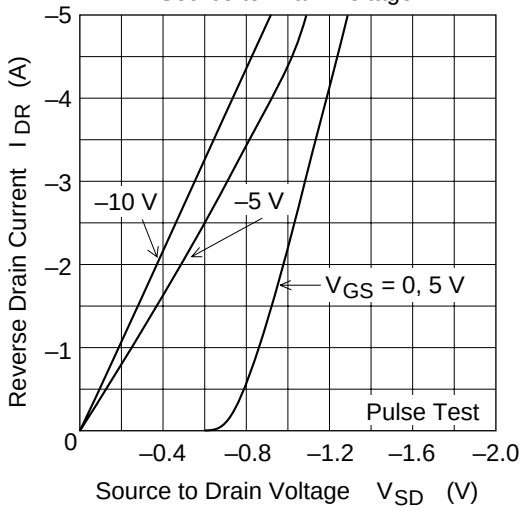
Dynamic Input Characteristics



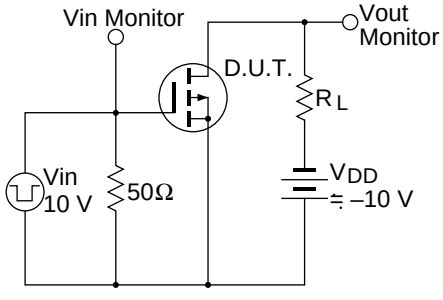
Switching Characteristics



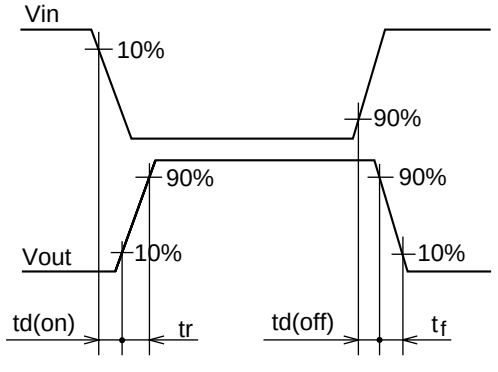
Reverse Drain Current vs.
Source to Drain Voltage



Switching Time Test Circuit



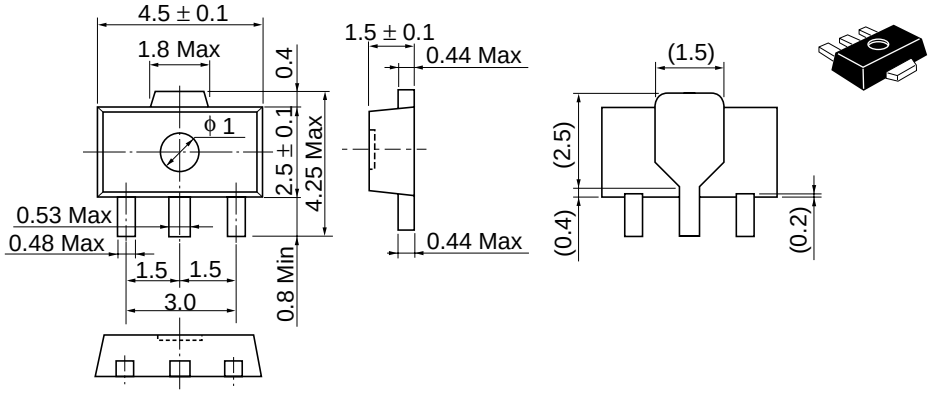
Switching Time Waveform



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.050 g

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