

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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# 2SJ486

## Silicon P Channel MOS FET Low Frequency Power Switching

# RENESAS

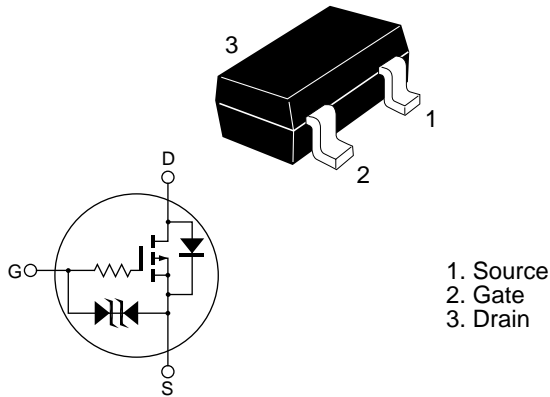
ADE-208-512A (Z)  
2nd. Edition  
Jul. 1997

### Features

- Low on-resistance  
 $R_{DS(on)} = 0.5 \Omega$  typ. (at  $V_{GS} = -4V$ ,  $I_D = -100$  mA)
- 2.5V gate drive devices.
- Small package (MPAK).

### Outline

MPAK



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-30	V
Gate to source voltage	$V_{GSS}$	±10	V
Drain current	$I_D$	-0.3	A
Drain peak current	$I_{D(pulse)}^{*1}$	-0.6	A
Channel dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

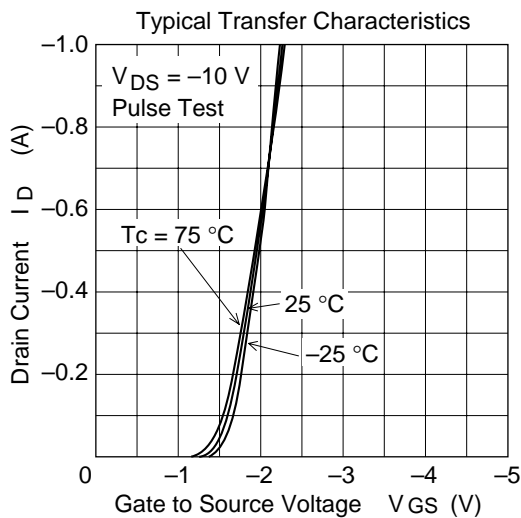
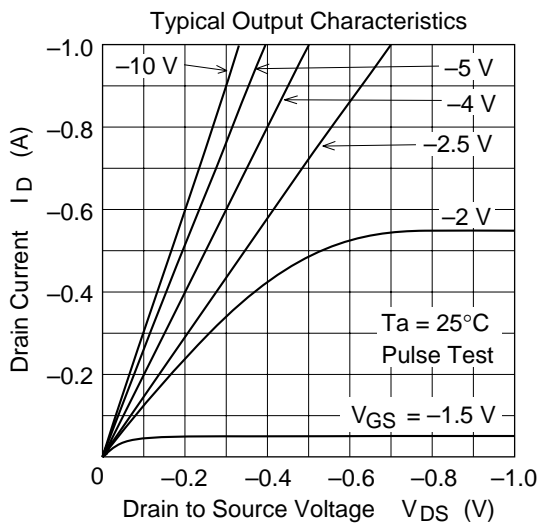
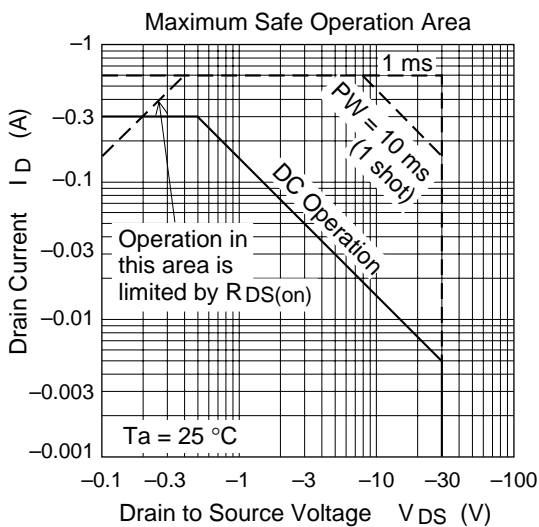
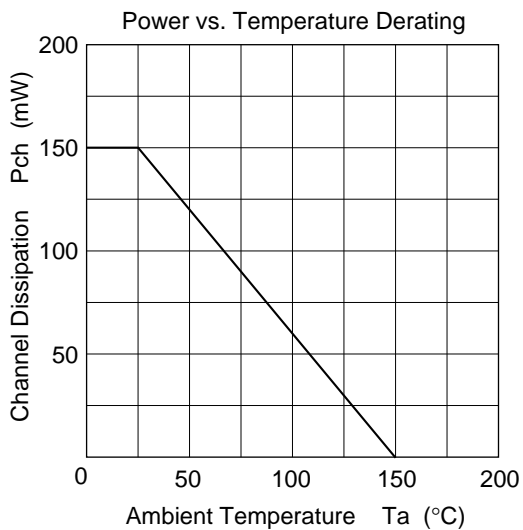
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %

## Electrical Characteristics (Ta = 25°C)

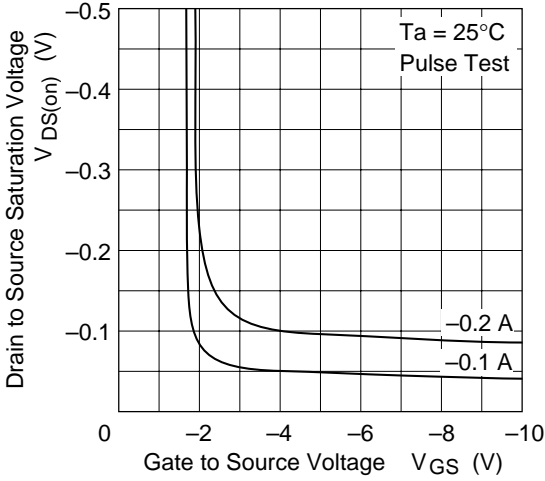
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10\mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	$I_G = \pm 100\mu A, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1.0	μA	$V_{DS} = -30 V, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±5.0	μA	$V_{GS} = \pm 6.5V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.5	—	-1.5	V	$I_D = -10\mu A, V_{DS} = -5V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.5	0.65	Ω	$I_D = -100mA$ $V_{GS} = -4V^{*1}$
	$R_{DS(on)}$	—	0.7	1.2	Ω	$I_D = -40mA$ $V_{GS} = -2.5V^{*1}$
Forward transfer admittance	$ y_{fs} $	0.4	0.65	—	S	$I_D = -100mA$ $V_{DS} = -10V^{*1}$
Input capacitance	Ciss	—	45	—	pF	$V_{DS} = -10V$
Output capacitance	Coss	—	76	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	5.4	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	120	—	ns	$V_{GS} = -4V$
Rise time	$t_r$	—	340	—	ns	$I_D = -150mA$
Turn-off delay time	$t_{d(off)}$	—	850	—	ns	$R_L = 66.6\Omega$
Fall time	$t_f$	—	550	—	ns	

Notes: 1. Pulse test  
2. Marking is "ZU-".

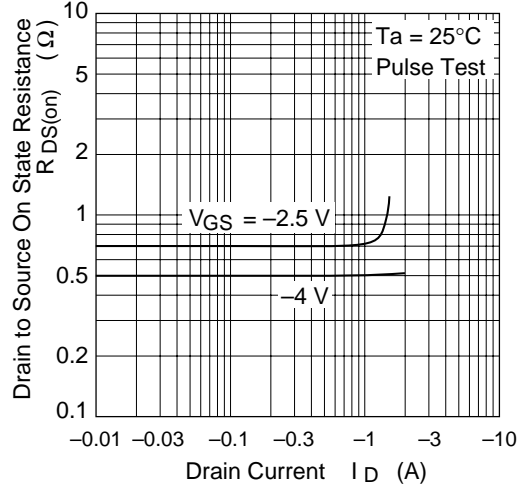
## Main Characteristics



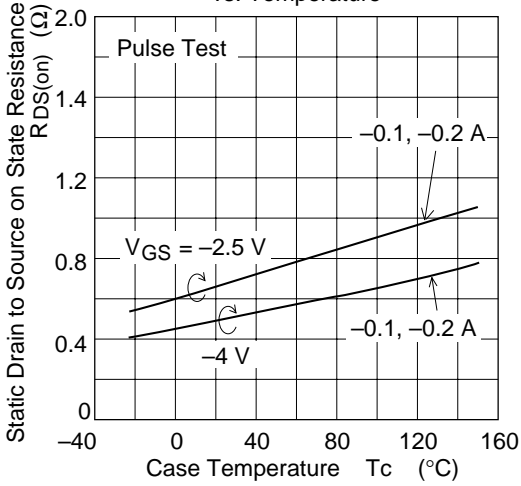
Drain to Source Saturation Voltage vs. Gate to Source Voltage



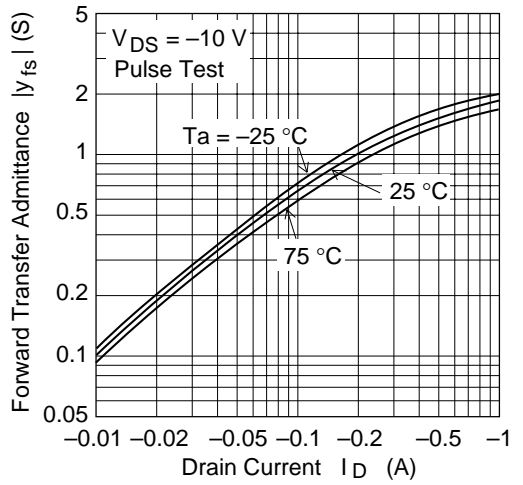
Static Drain to Source on State Resistance vs. Drain Current



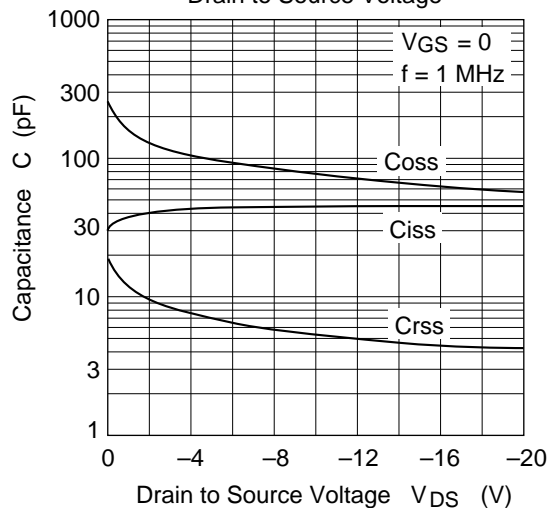
Static Drain to Source on State Resistance vs. Temperature



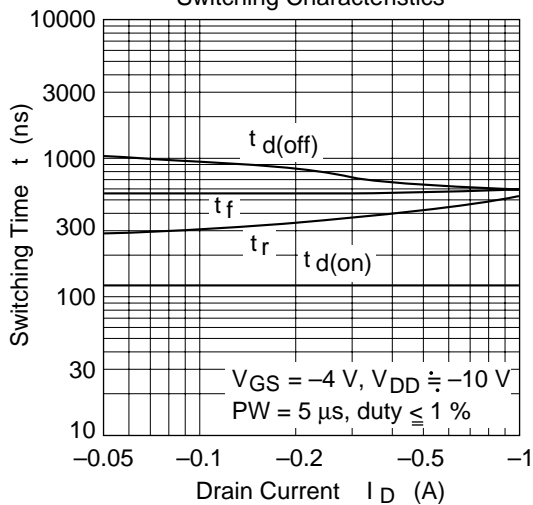
Forward Transfer Admittance vs. Drain Current



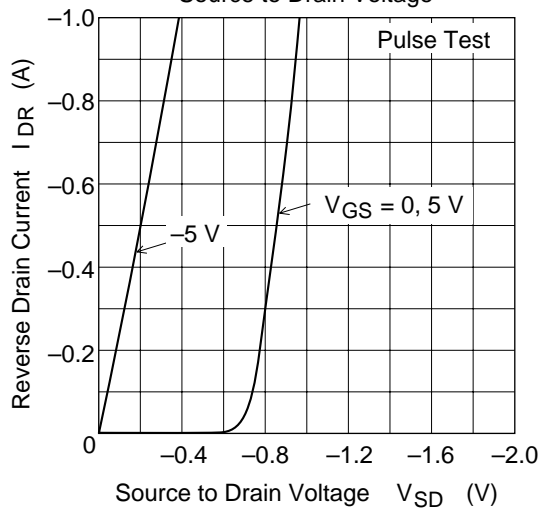
Typical Capacitance vs. Drain to Source Voltage

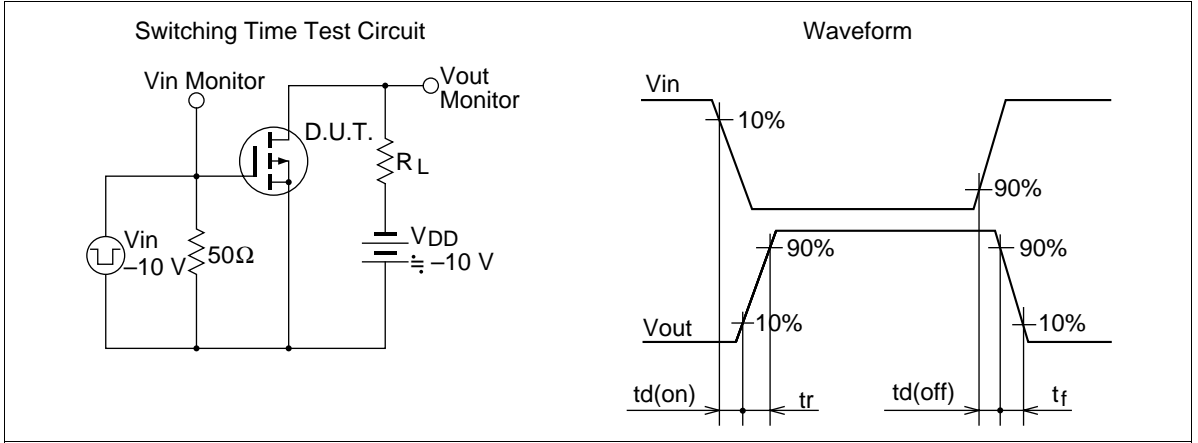


Switching Characteristics



Reverse Drain Current vs. Source to Drain Voltage

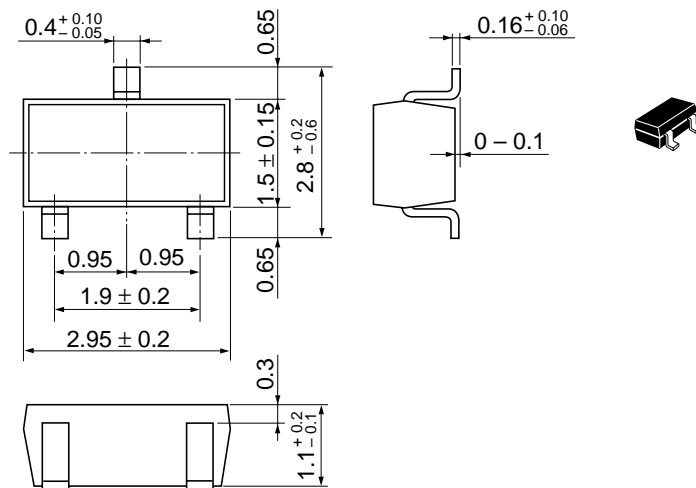




## Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	MPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.011 g

## Cautions

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