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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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2SJ518

Silicon P Channel MOS FET
High Speed Power Switching

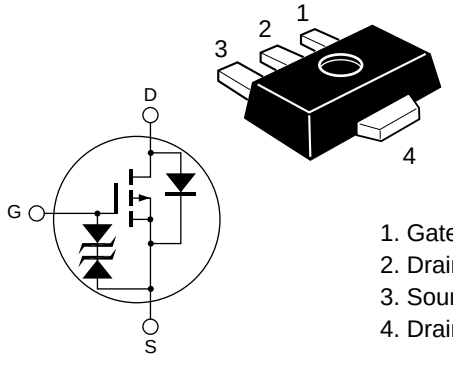
ADE-208-580B (Z)
3rd. Edition
Jul. 1998

Features

- Low on-resistance
  $R_{DS(on)}$ = 0.35 Ω typ. at (V_{GS} = –10V, I_D = –1A)
- Low drive current
- 4 V gete drive devices
- High speed switching

Outline

UPAK



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–2	A
Drain peak current	$I_{D(pulse)}$ Note1	–4	A
Body-drain diode reverse drain current	I_{DR}	–2	A
Avalenche current	I_{AP} Note2	–2	A
Avalenche energy	E_{AR}	0.34	mJ
Channel dissipation	Pch Note3	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

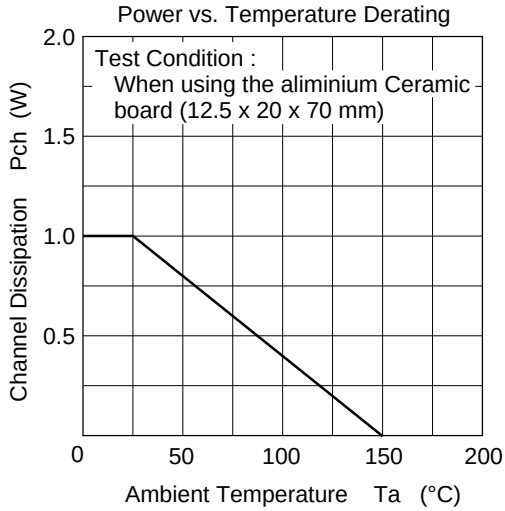
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. value at Tch = 25°C, Rg ≥ 50 Ω
3. Value at when using the aluminaceramic board (12.5x20x0.7mm)

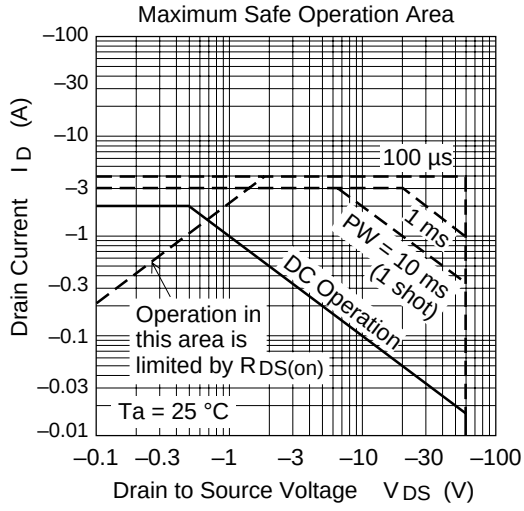
Electrical Characteristics (Ta = 25°C)

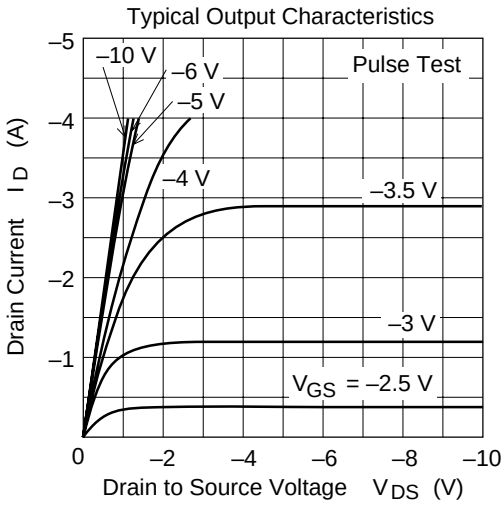
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –60 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1mA, V_{DS} = –10V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.35	0.46	Ω	I_D = –1A, V_{GS} = –10V Note4
	$R_{DS(on)}$	—	0.45	0.63	Ω	I_D = –1A, V_{GS} = –4V Note4
Forward transfer admittance	$\|y_{fs}\|$	1.2	2.0	—	S	I_D = –1A, V_{DS} = –10V Note4
Input capacitance	Ciss	—	220	—	pF	V_{DS} = –10V
Output capacitance	Coss	—	110	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	35	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	V_{GS} = –10V, I_D = –1A
Rise time	t_r	—	11	—	ns	R_L = 30Ω
Turn-off delay time	$t_{d(off)}$	—	45	—	ns	
Fall time	t_f	—	30	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.05	—	V	I_D = –2A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	50	—	ns	I_F = –2A, V_{GS} = 0 diF/ dt = 50A/µs

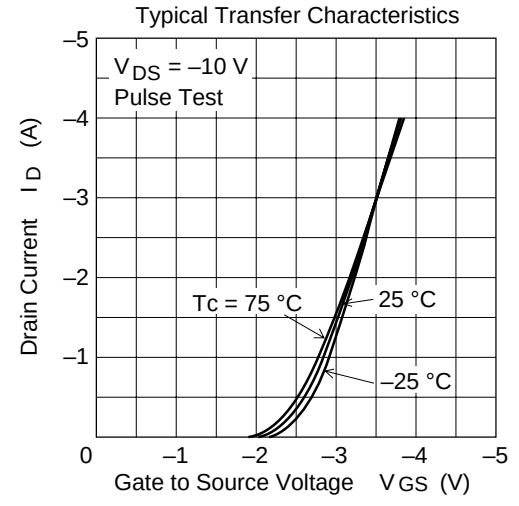
Note: 4. Pulse test
5. Marking is “AZ”

Main Characteristics

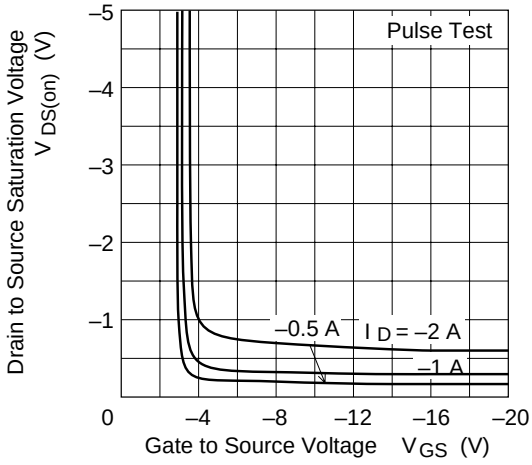




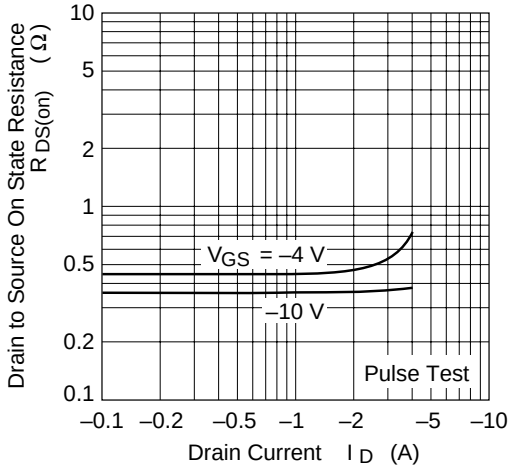




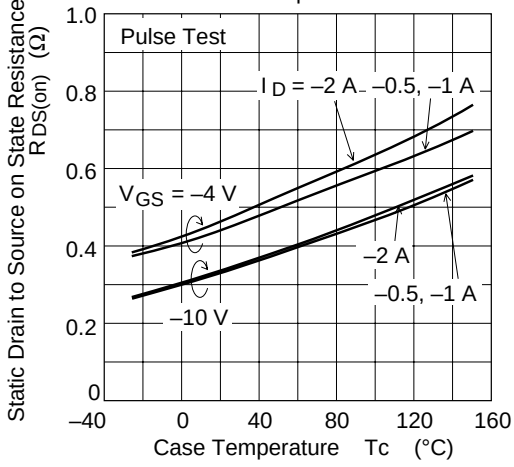
Drain to Source Saturation Voltage vs. Gate to Source Voltage



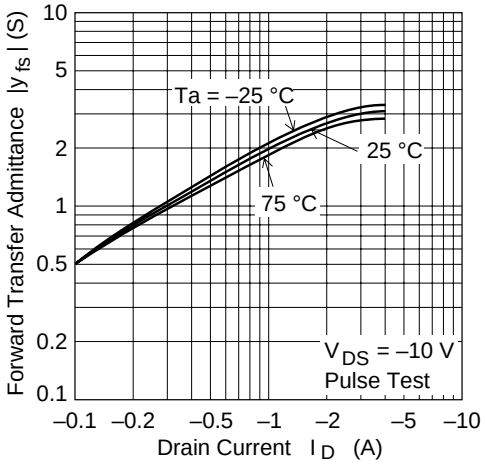
Static Drain to Source on State Resistance vs. Drain Current



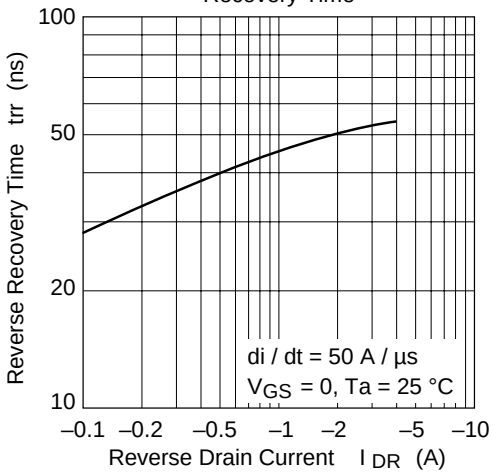
Static Drain to Source on State Resistance vs. Temperature



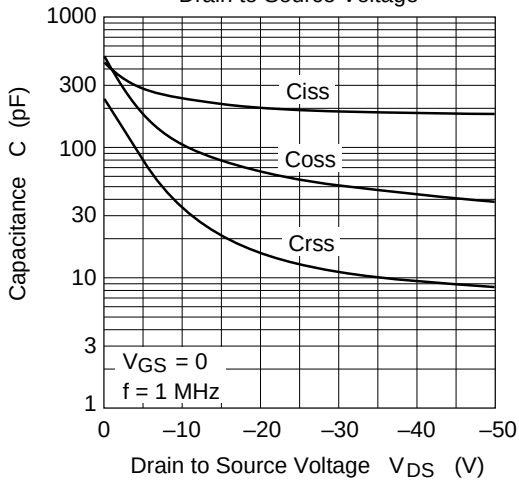
Forward Transfer Admittance vs. Drain Current



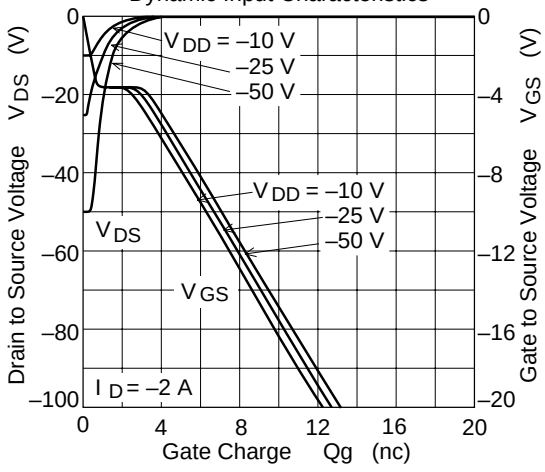
Body–Drain Diode Reverse Recovery Time



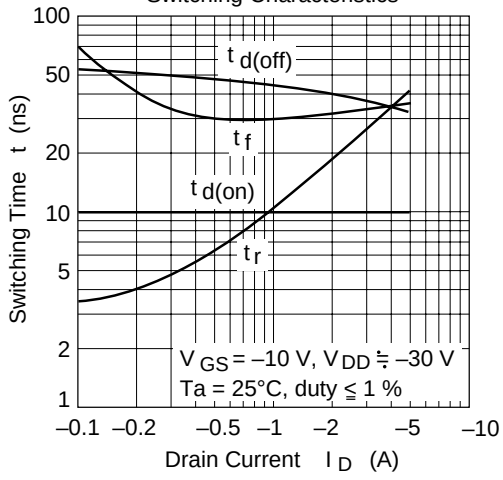
Typical Capacitance vs. Drain to Source Voltage



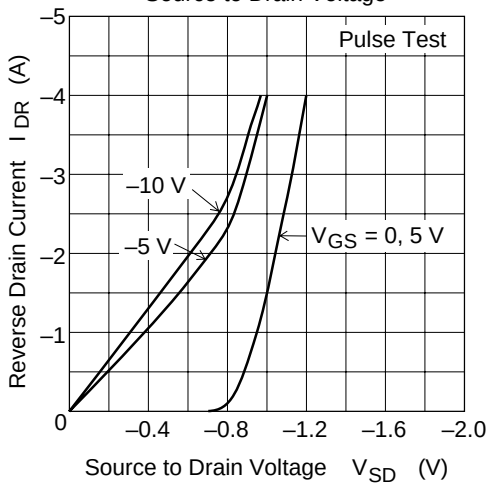
Dynamic Input Characteristics



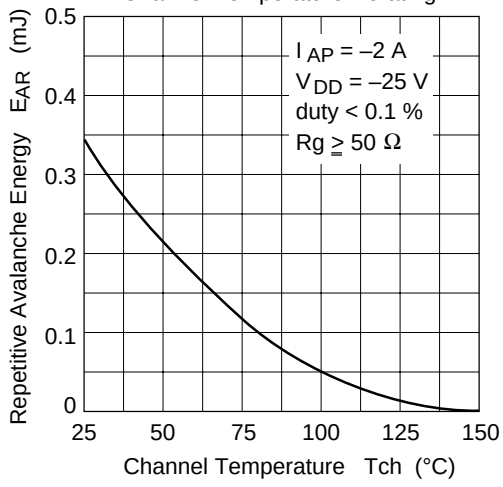
Switching Characteristics



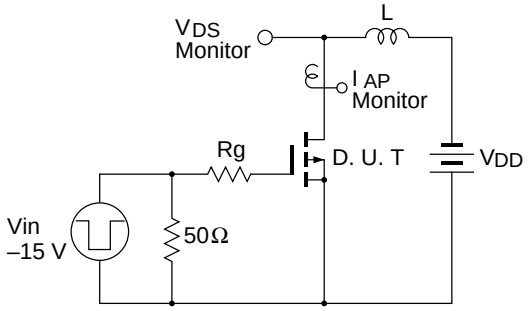
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

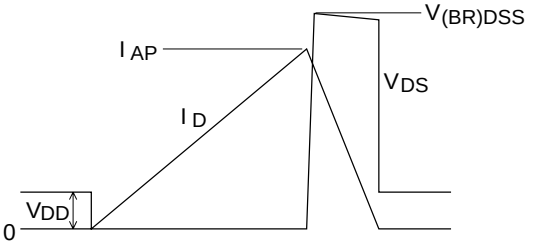


Avalanche Test Circuit

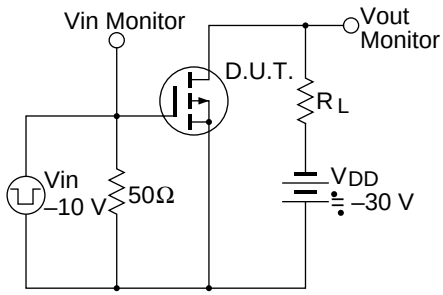


Avalanche Waveform

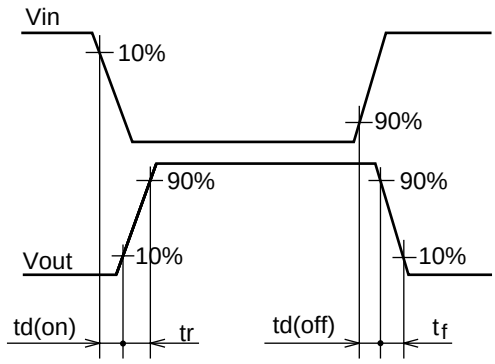
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



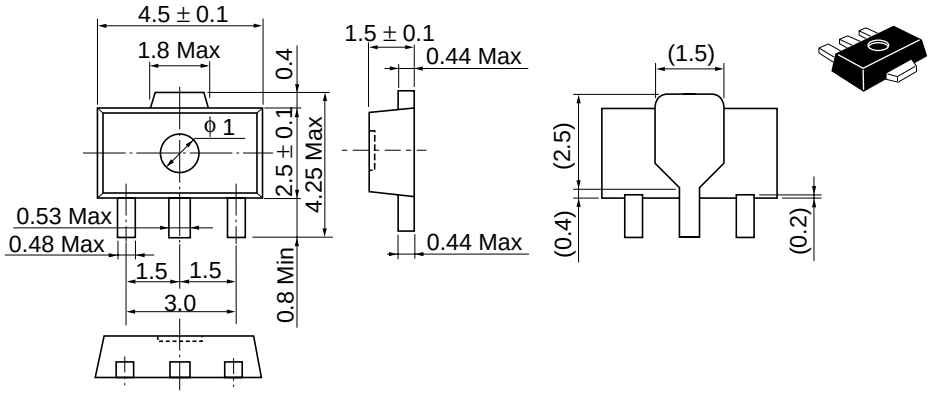
Waveform



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.050 g

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