

To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SJ554

Silicon P Channel MOS FET High Speed Power Switching

RENESAS

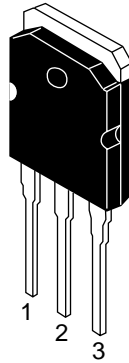
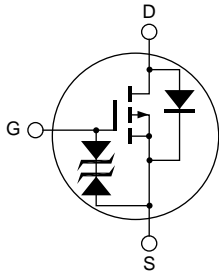
ADE-208-628B (Z)
3rd. Edition
Jun. 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.028\Omega$ typ.
- Low drive current.
- 4V gate drive devices.
- High speed switching.

Outline

TO-3P



1. Gate
2. Drain
(Flange)
3. Source

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	-60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	-45	A
Drain peak current	I _{D(pulse)} ^{Note1}	-180	A
Body-drain diode reverse drain current	I _{DR}	-45	A
Avalanche current	I _{AP} ^{Note3}	-45	A
Avalanche energy	E _{AR} ^{Note3}	173	mJ
Channel dissipation	Pch ^{Note2}	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

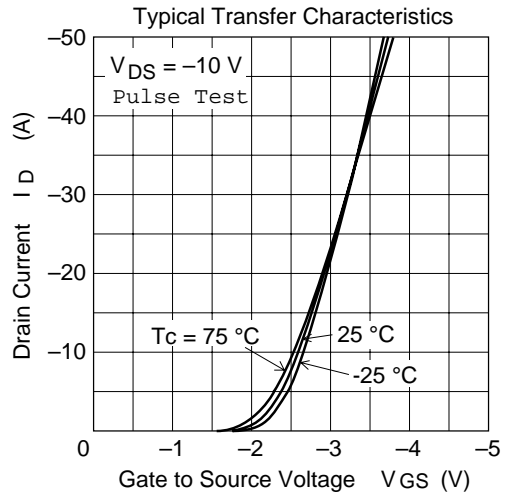
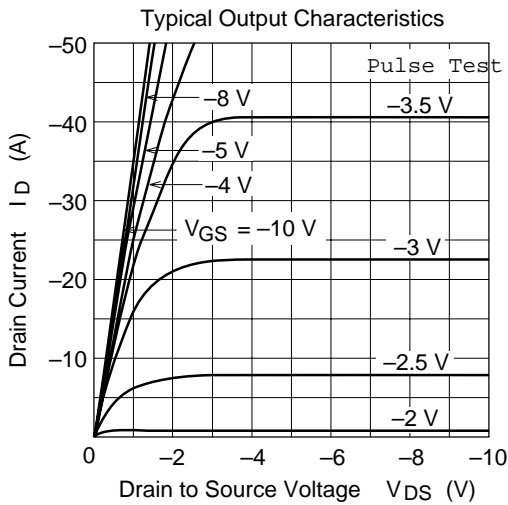
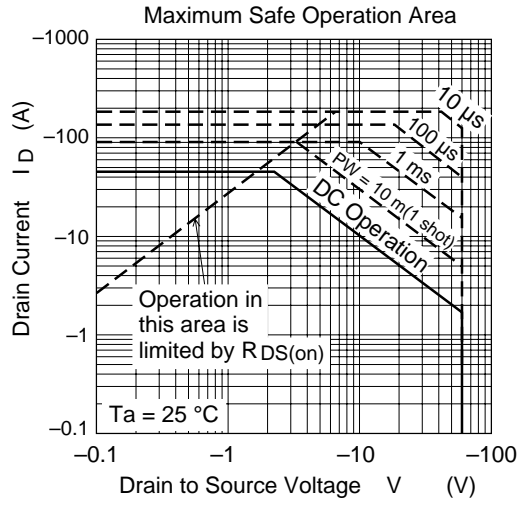
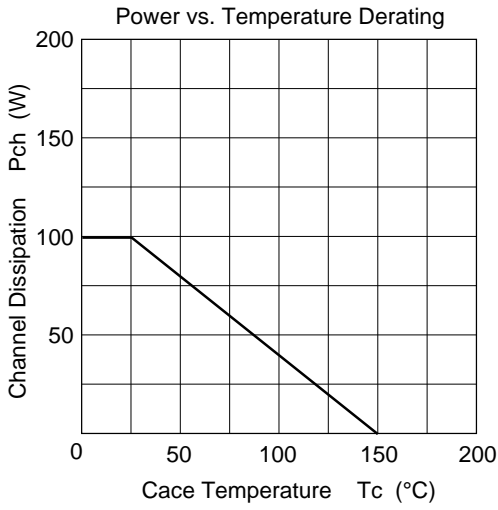
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

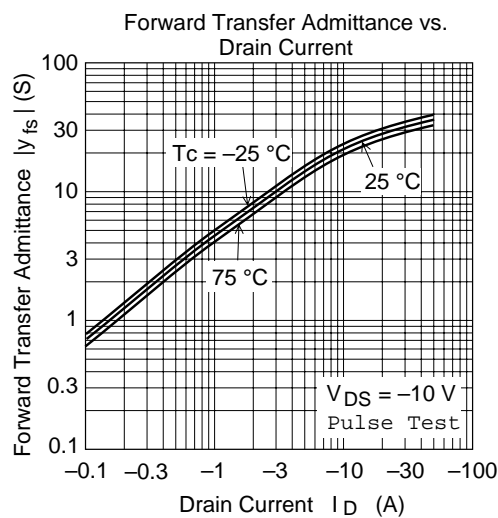
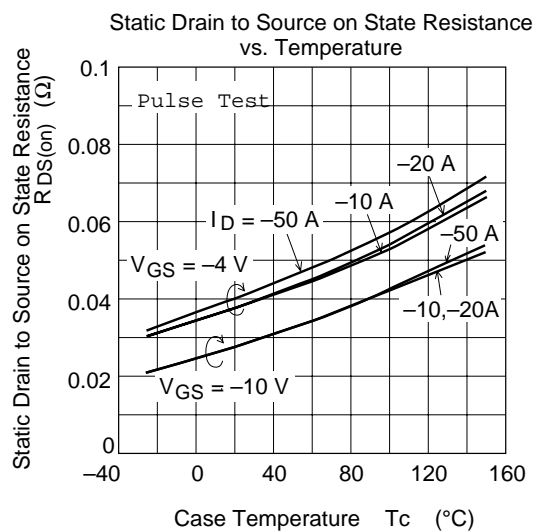
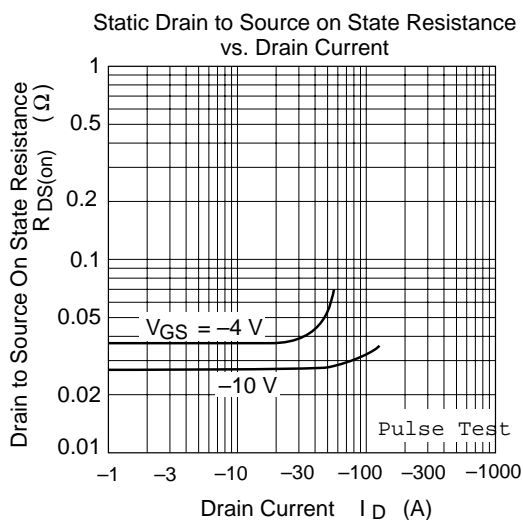
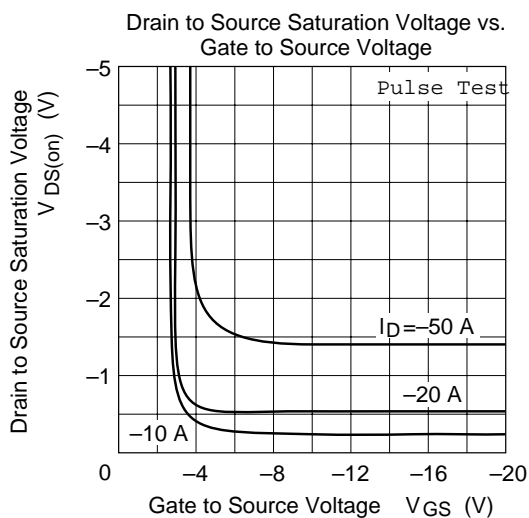
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1\text{mA}$, $V_{DS} = -10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.028	0.037	Ω	$I_D = -25\text{A}$, $V_{GS} = -10\text{V}$ ^{Note4}
	$R_{DS(on)}$	—	0.038	0.055	Ω	$I_D = -25\text{A}$, $V_{GS} = -4\text{V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	18	30	—	S	$I_D = -25\text{A}$, $V_{DS} = -10\text{V}$ ^{Note4}
Input capacitance	C_{iss}	—	2500	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	C_{oss}	—	1300	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	300	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	$V_{GS} = -10\text{V}$, $I_D = -25\text{A}$
Rise time	t_r	—	160	—	ns	$R_L = 1.2\Omega$
Turn-off delay time	$t_{d(off)}$	—	350	—	ns	
Fall time	t_f	—	240	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-1.1	—	V	$I_F = -45\text{A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	100	—	ns	$I_F = -45\text{A}$, $V_{GS} = 0$ $diF/dt = 50\text{A}/\mu\text{s}$

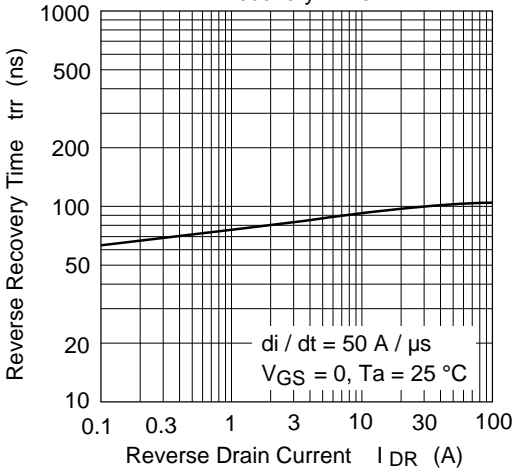
Note: 4. Pulse test

Main Characteristics

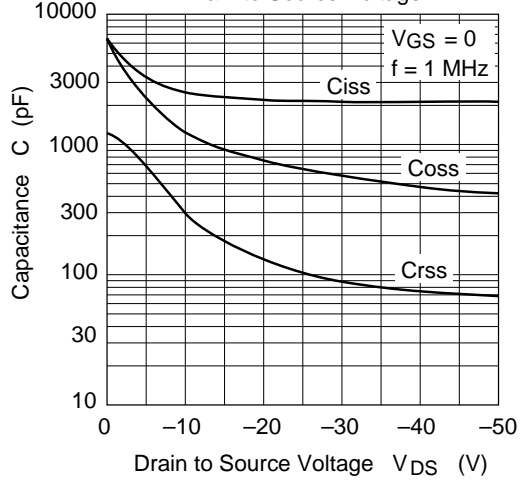




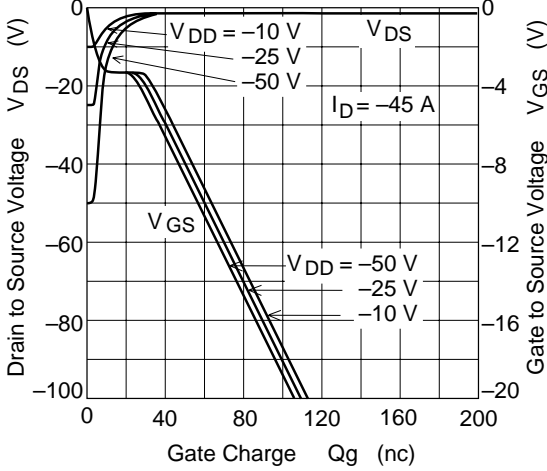
Body-Drain Diode Reverse Recovery Time



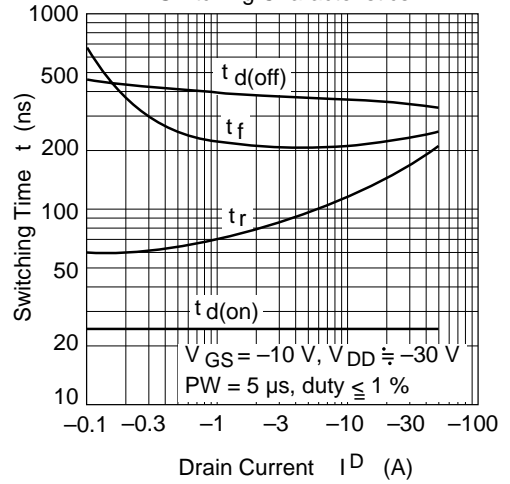
Typical Capacitance vs. Drain to Source Voltage

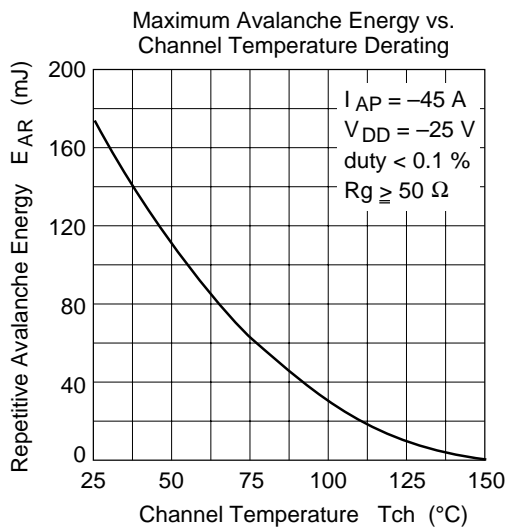
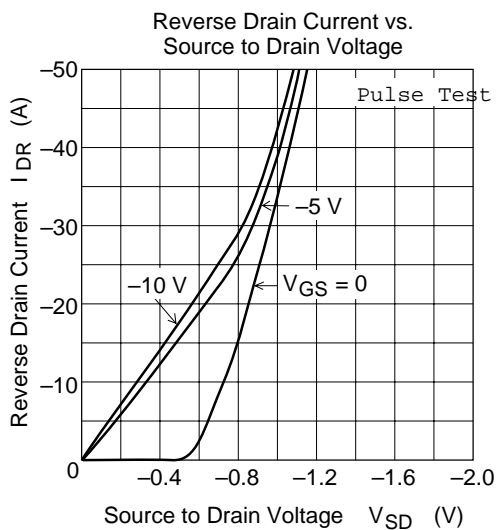


Dynamic Input Characteristics

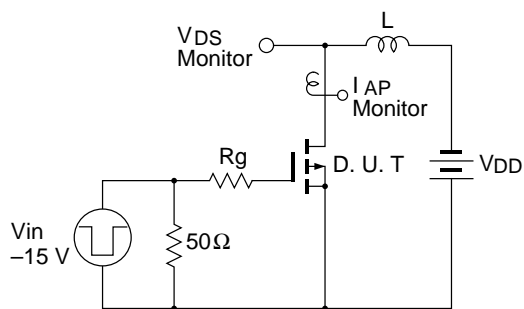


Switching Characteristics



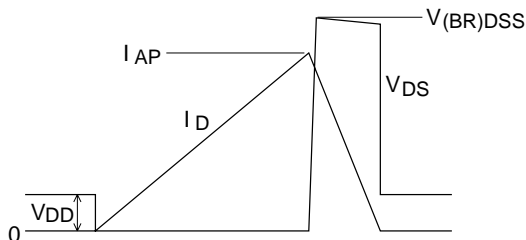


Avalanche Test Circuit

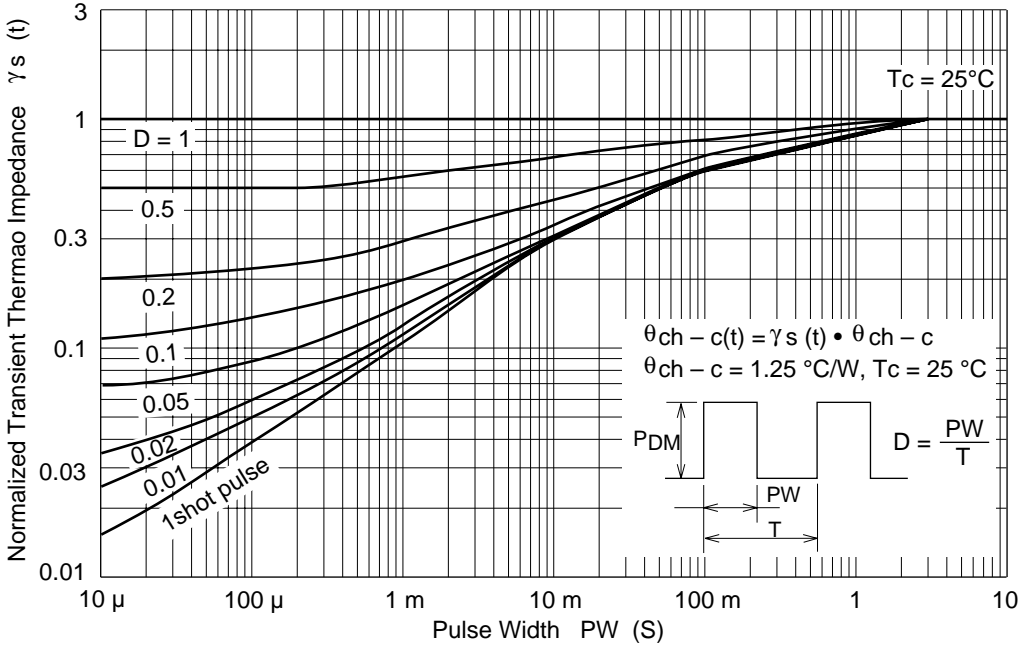


Avalanche Waveform

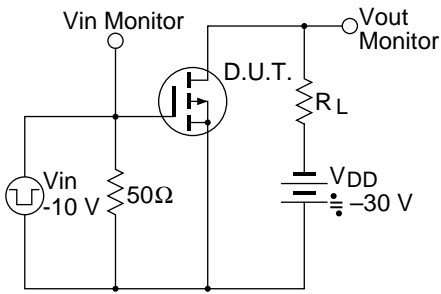
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



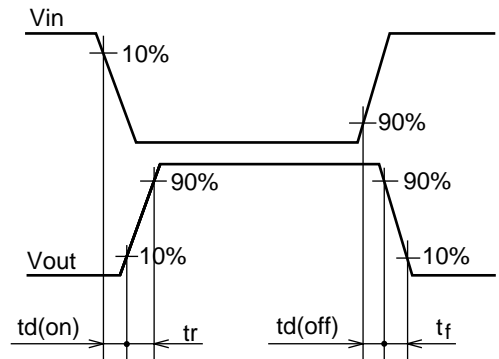
Normalized Transient Thermal Impedance vs. Pulse Width



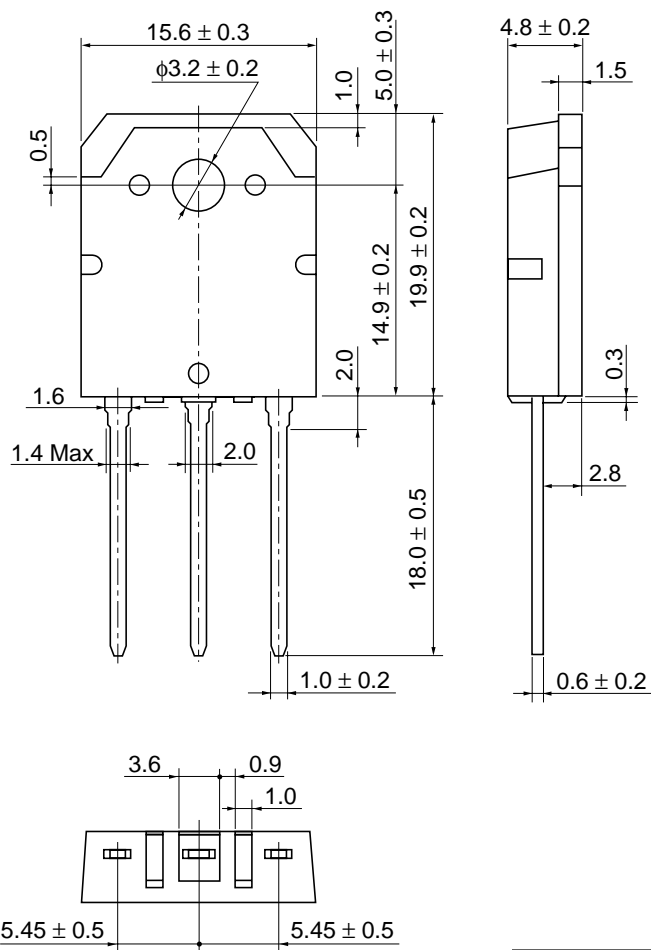
Switching Time Test Circuit



Waveform

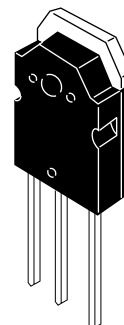


Package Dimensions



As of January, 2001

Unit: mm



Hitachi Code	TO-3P
JEDEC	—
EIAJ	Conforms
Mass (reference value)	5.0 g

Cautions

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