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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2554

Silicon N-Channel MOS FET

RENESAS

ADE-208-359D (Z)
5th. Edition
Aug. 1995

Application

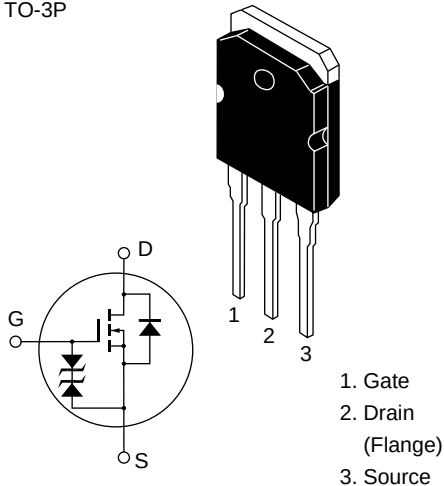
High speed power switching

Features

- Low on-resistance
- $R_{DS(on)} = 4.5 \text{ m}\Omega$ typ.
- High speed switching
- 4 V gate drive device can be driven from 5 V source

Outline

TO-3P



Absolute Maximum Ratings (Ta = 25°C)

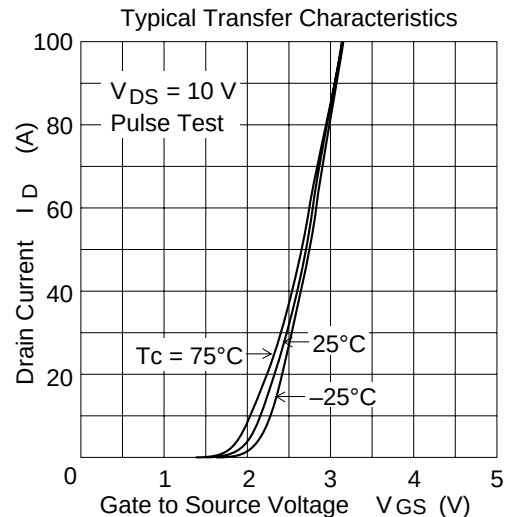
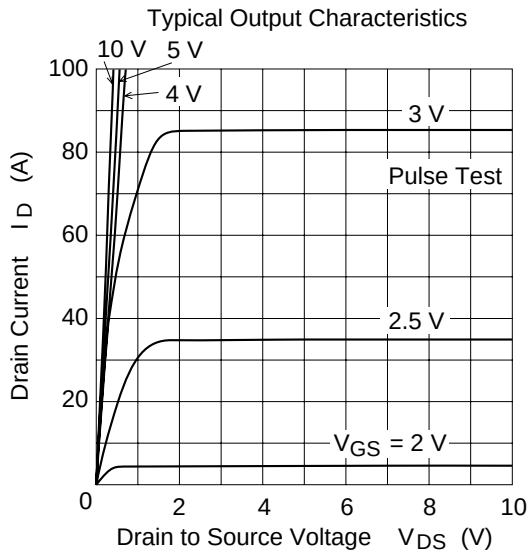
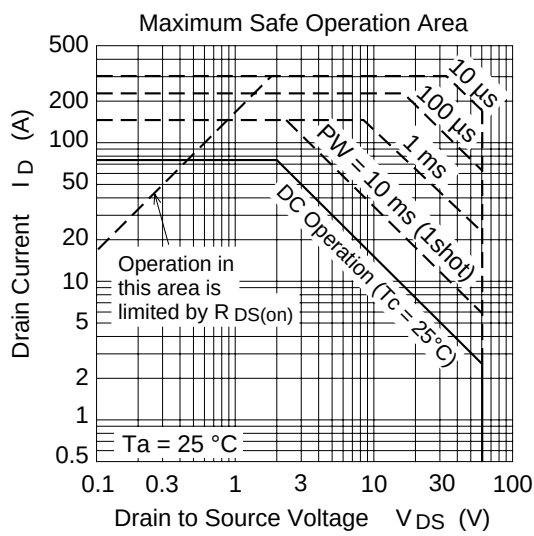
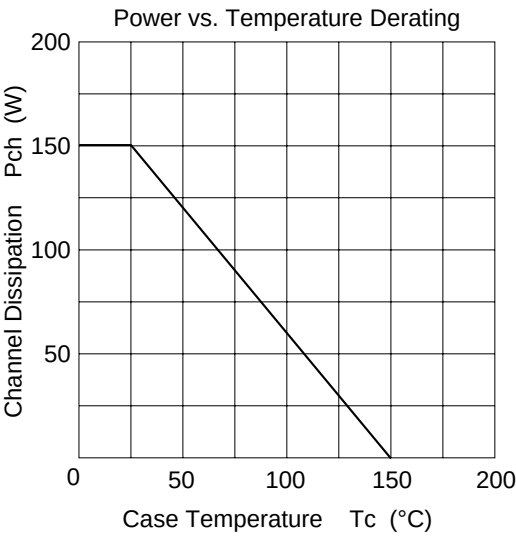
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	75	A
Drain peak current	$I_{D(pulse)}^{*1}$	300	A
Body to drain diode reverse drain current	I_{DR}^{*2}	75	A
Avalanche current	I_{AP}^{*3}	50	A
Avalanche energy	E_{AR}^{*3}	214	mJ
Channel dissipation	P_{ch}^{*2}	150	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

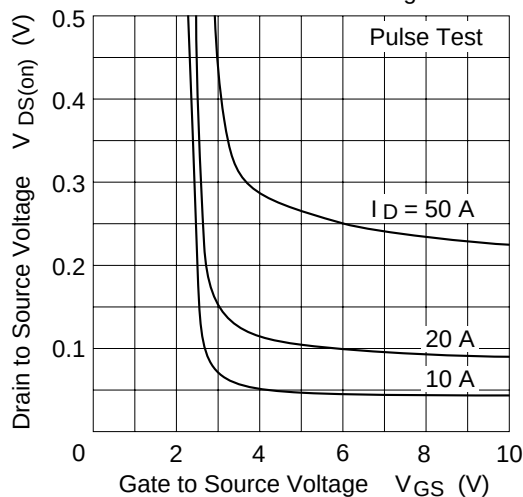
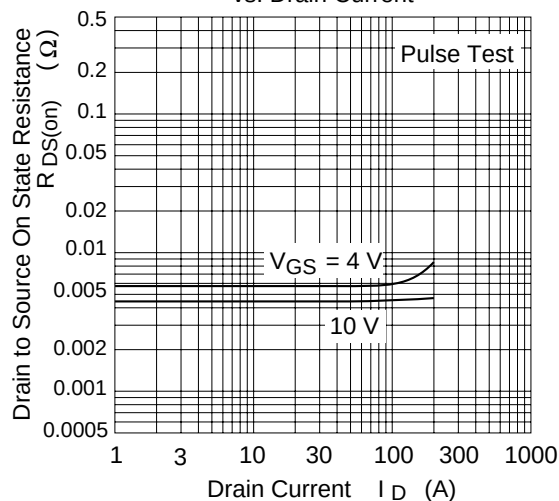
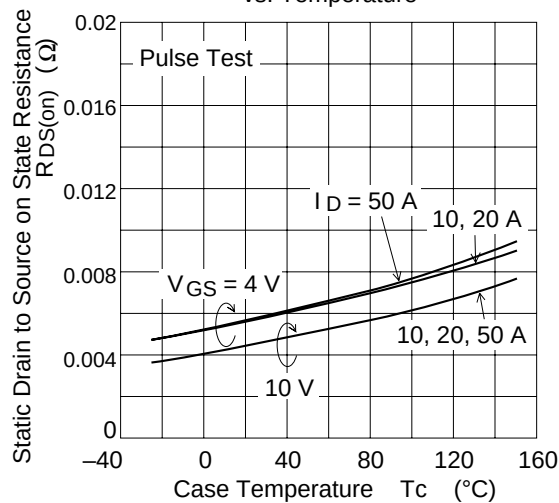
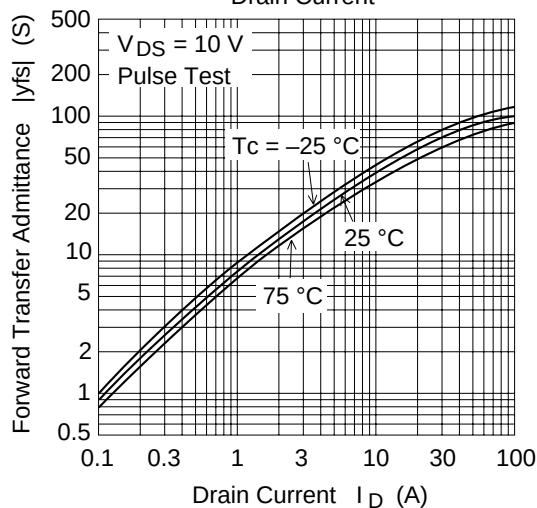
Notes: 1. PW 10 μs, duty cycle 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg 50 Ω

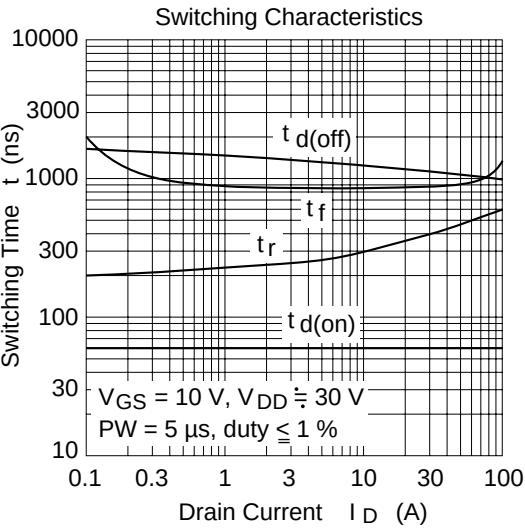
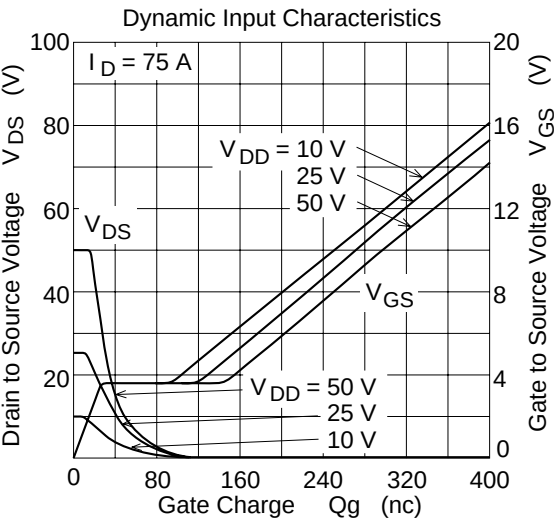
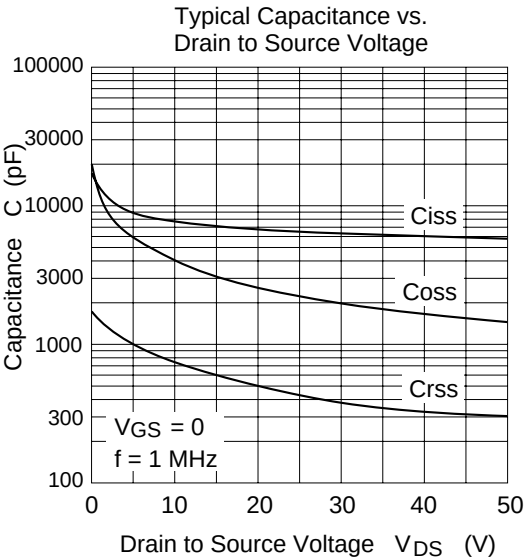
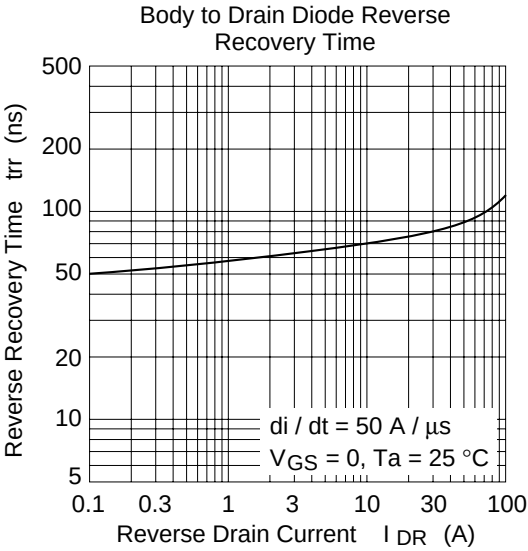
Electrical Characteristics (Ta = 25°C)

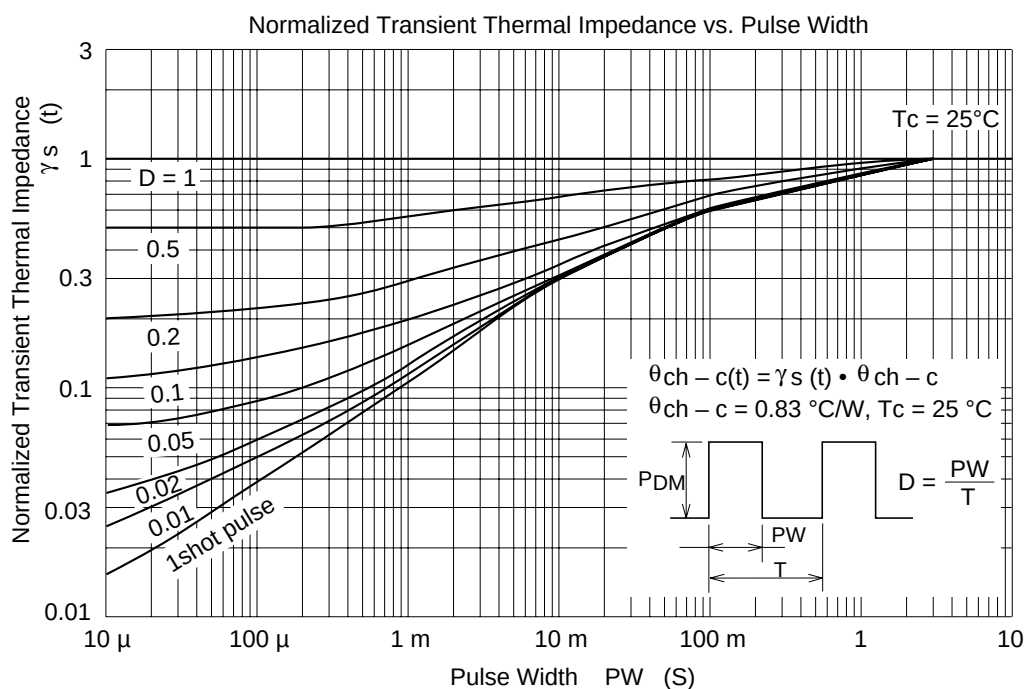
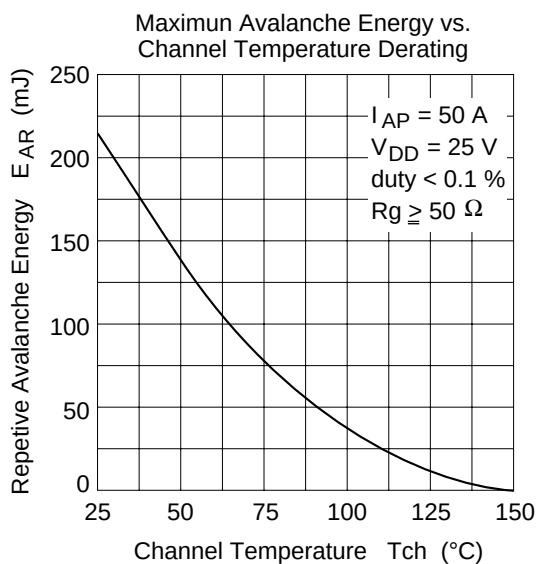
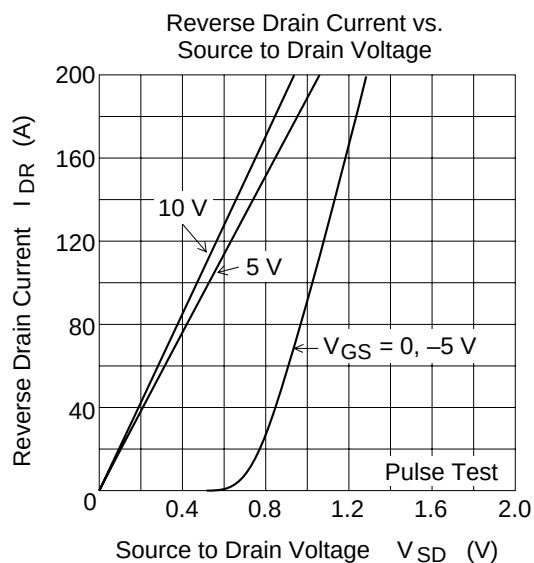
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	100	μA	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.5	6	m	$I_D = 40 \text{ A}$ $V_{GS} = 10 \text{ V}^{*1}$
		—	5.8	10	m	$I_D = 40 \text{ A}$ $V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	50	80	—	S	$I_D = 40 \text{ A}$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	7700	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	4100	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	760	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	60	—	ns	$I_D = 40 \text{ A}$
Rise time	t_r	—	420	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	1200	—	ns	$R_L = 0.75 \text{ }\Omega$
Fall time	t_f	—	900	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.95	—	V	$I_F = 75 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	105	—	ns	$I_F = 75 \text{ A}$, $V_{GS} = 0$ $diF / dt = 50 \text{ A} / \mu\text{s}$

Note: 1. Pulse Test



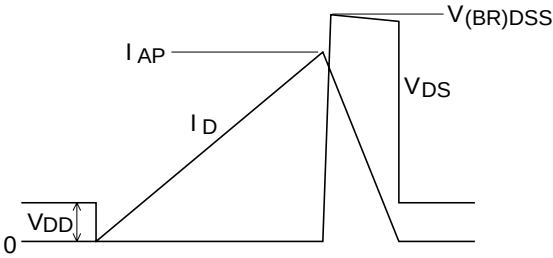
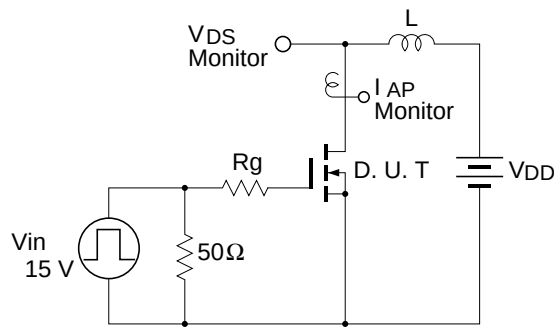
Drain to Source Saturation Voltage vs.
Gate to Source VoltageStatic Drain to Source on State Resistance
vs. Drain CurrentStatic Drain to Source on State Resistance
vs. TemperatureForward Transfer Admittance vs.
Drain Current



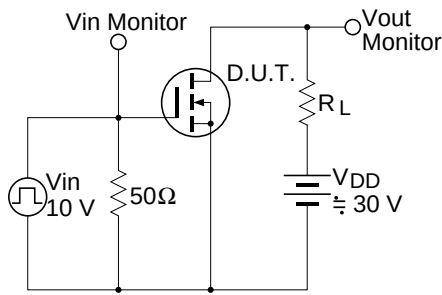


Avalanche Test Circuit and Waveform

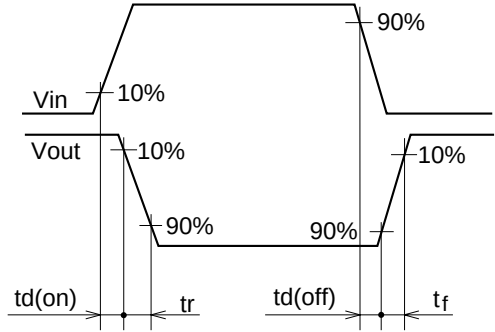
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



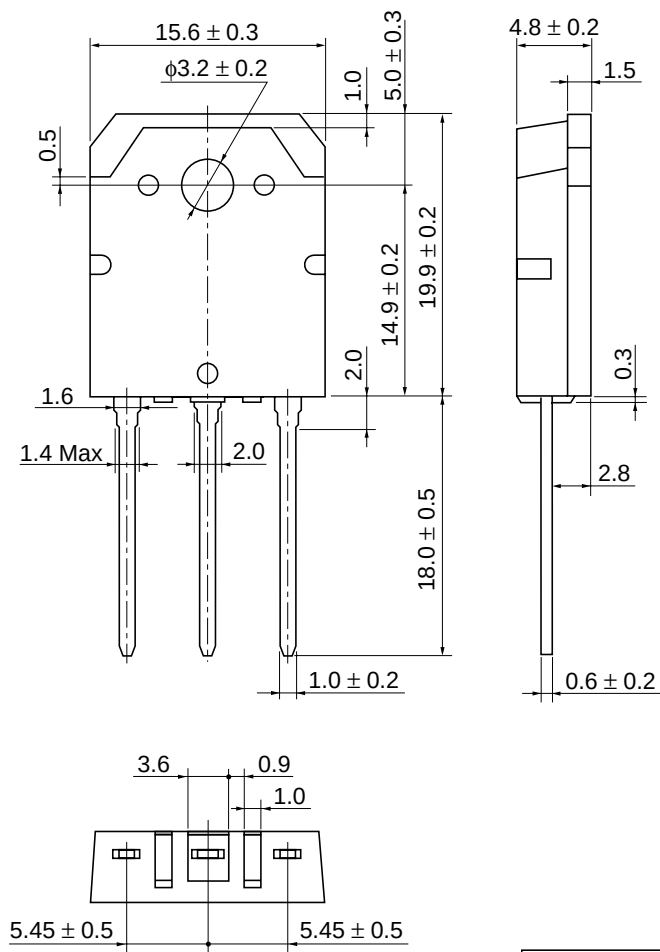
Switching Time Test Circuit



Waveform

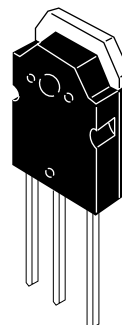


Package Dimensions



As of January, 2001

Unit: mm



Hitachi Code	TO-3P
JEDEC	—
EIAJ	Conforms
Mass (reference value)	5.0 g

Cautions

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