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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2729

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

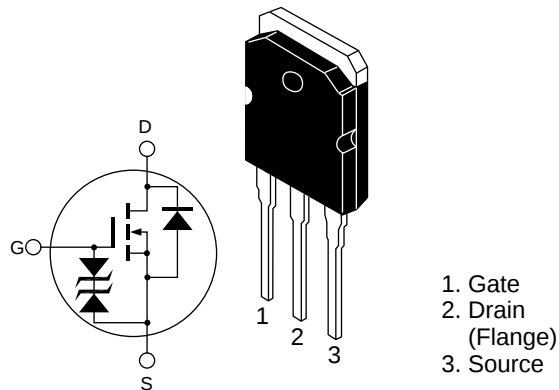
ADE-208-455A (Z)
2nd. Edition
Mar. 2001

Features

- Low on-resistance
- High speed switching
- Low drive current
- Avalanche ratings

Outline

TO-3P



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}^{*1}$	80	A
Body to drain diode reverse drain current	I_{DR}	20	A
Avalanche current	I_{AP}^{*3}	20	A
Avalanche energy	E_{AR}^{*3}	22	mJ
Channel dissipation	Pch^{*2}	150	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

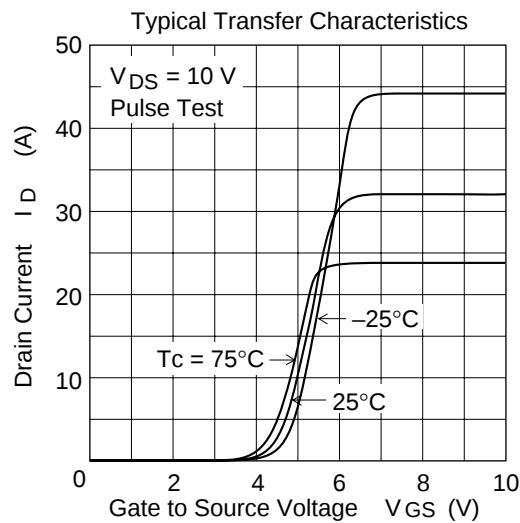
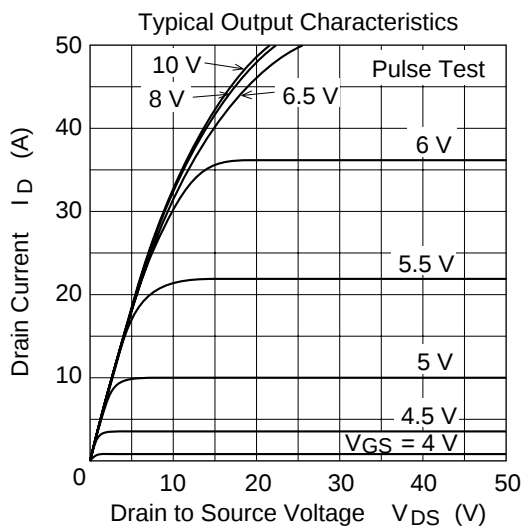
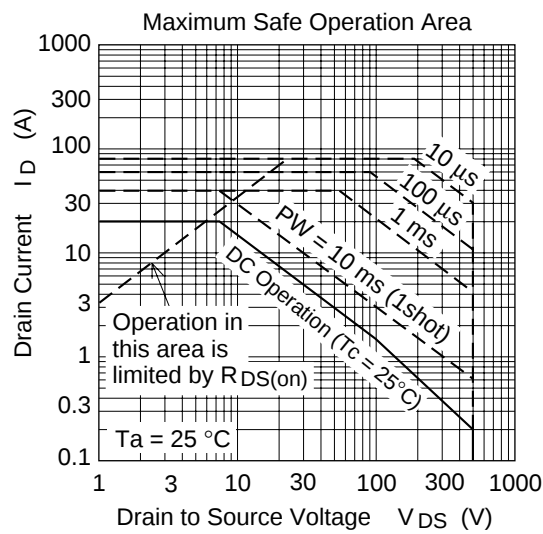
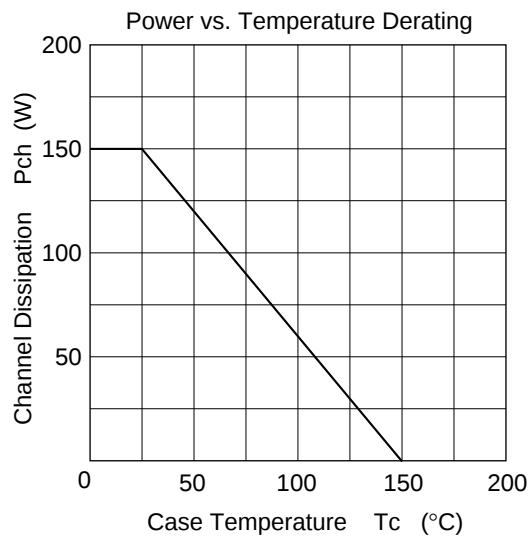
Notes: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg $\geq 50\Omega$

Electrical Characteristics (Ta = 25°C)

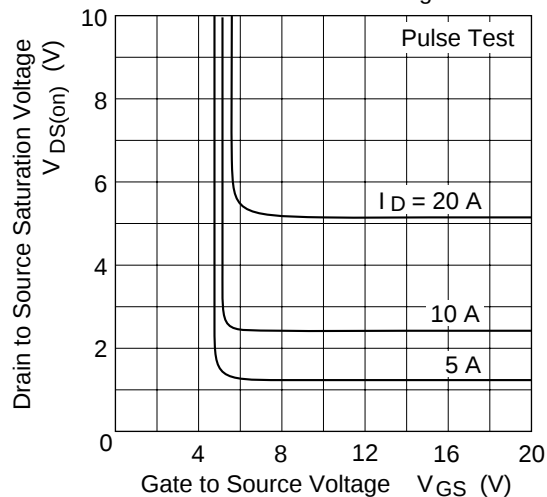
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 25\text{V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 500\text{V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.5	—	3.5	V	$I_D = 1\text{mA}$, $V_{DS} = 10\text{V}^{*1}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.24	0.29	Ω	$I_D = 10\text{A}$, $V_{GS} = 10\text{V}^{*1}$
Forward transfer admittance	$ y_{fs} $	9	15	—	S	$I_D = 10\text{A}$, $V_{DS} = 10\text{V}^{*1}$
Input capacitance	C_{iss}	—	3300	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	C_{oss}	—	900	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	120	—	pF	$f = 1\text{MHz}$
Total gate charge	Q_g	—	55	—	nc	$V_{DD} = 400\text{V}$
Gate to source charge	Q_{gs}	—	14	—	nc	$V_{GS} = 10\text{V}$
Gate to drain charge	Q_{gd}	—	17	—	nc	$I_D = 20\text{A}$
Turn-on delay time	$t_{d(on)}$	—	45	—	ns	$V_{GS} = 10\text{V}$, $I_D = 10\text{A}$
Rise time	t_r	—	140	—	ns	$R_L = 3\Omega$
Turn-off delay time	$t_{d(off)}$	—	150	—	ns	
Fall time	t_f	—	85	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.0	—	V	$I_D = 20\text{A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	400	—	ns	$I_F = 20\text{A}$, $V_{GS} = 0$ $diF/dt = 100\text{A}/\mu\text{s}$

Note: 1. Pulse test

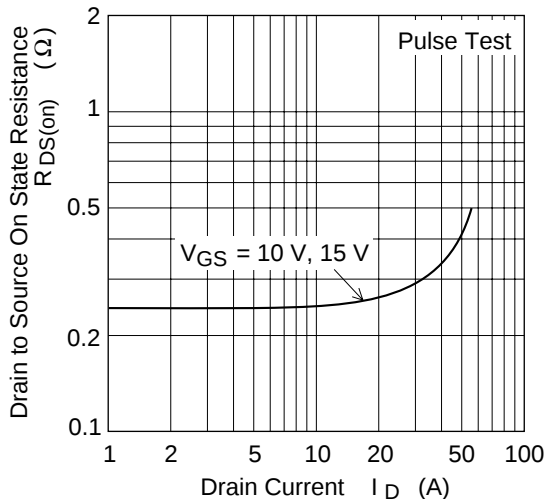
Main Characteristics



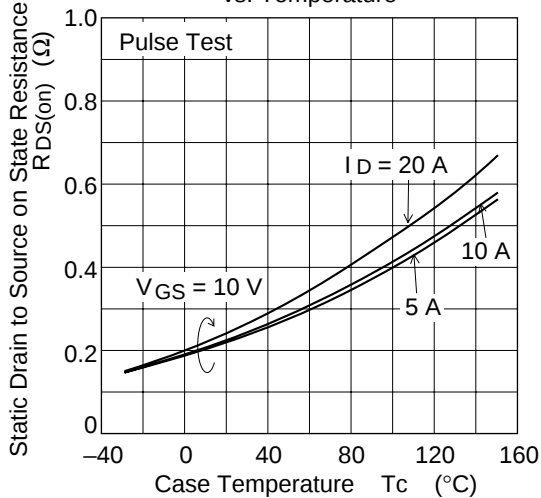
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



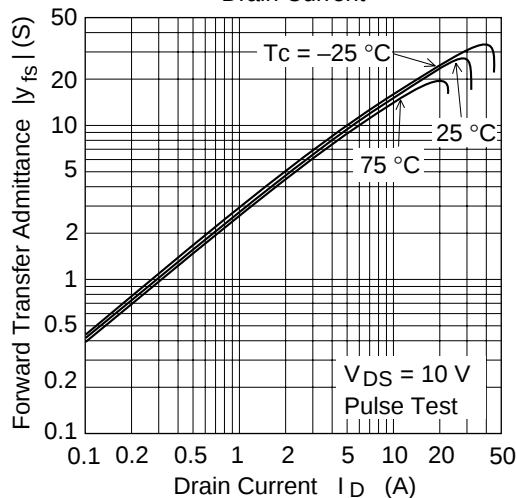
Static Drain to Source on State Resistance
vs. Drain Current



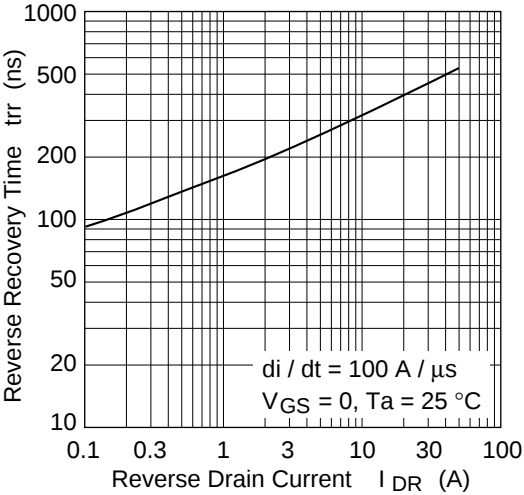
Static Drain to Source on State Resistance
vs. Temperature



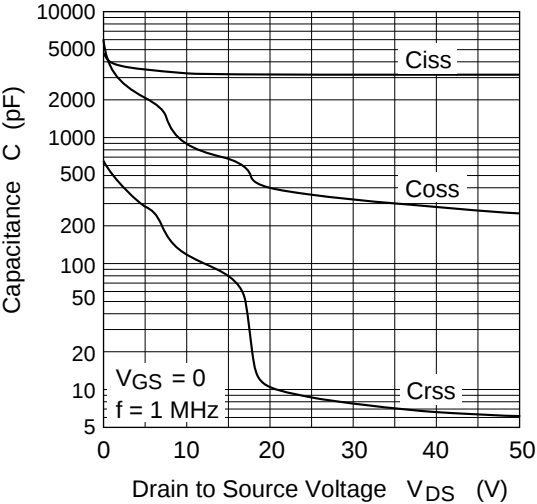
Forward Transfer Admittance vs.
Drain Current



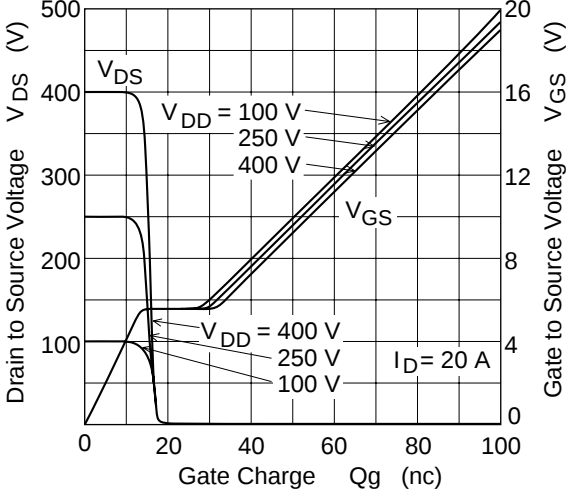
Body to Drain Diode Reverse Recovery Time



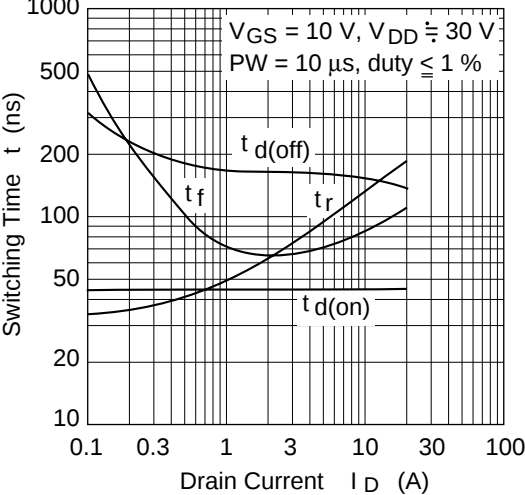
Typical Capacitance vs. Drain to Source Voltage

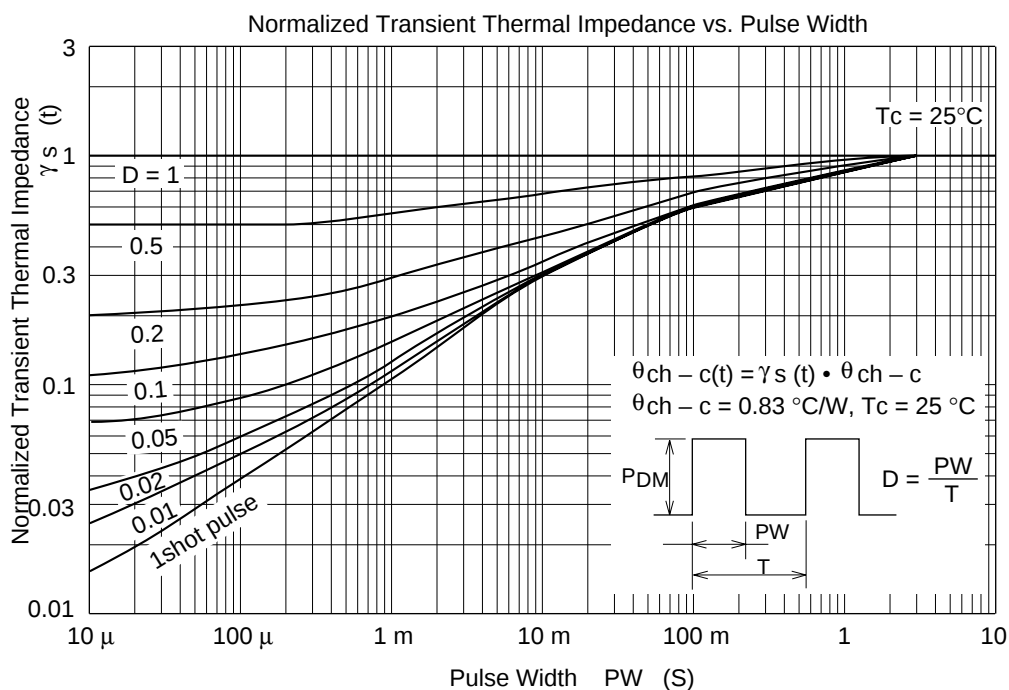
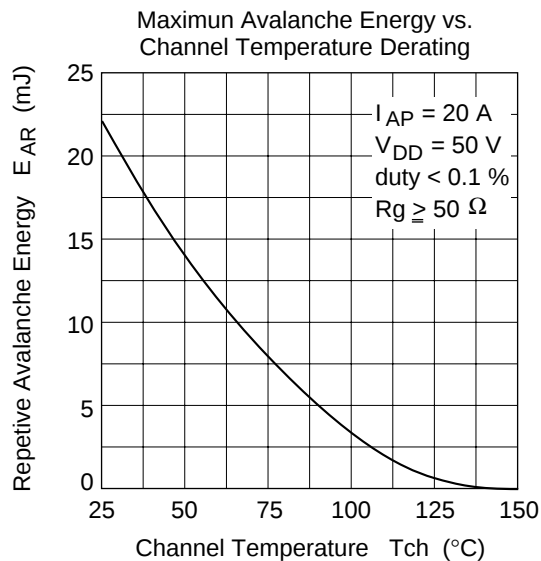
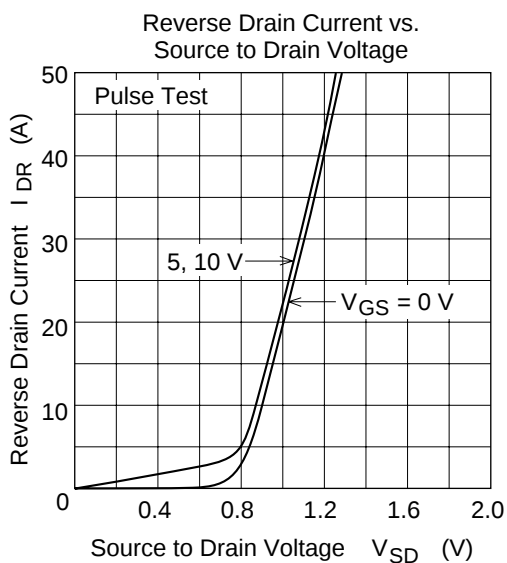


Dynamic Input Characteristics

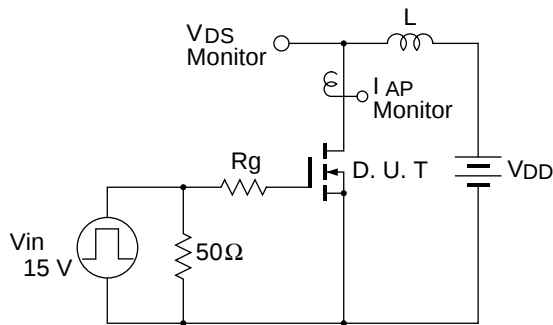


Switching Characteristics

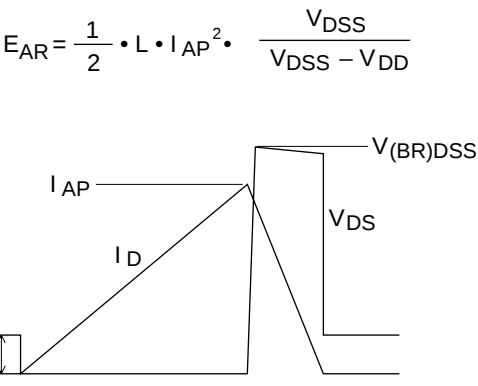




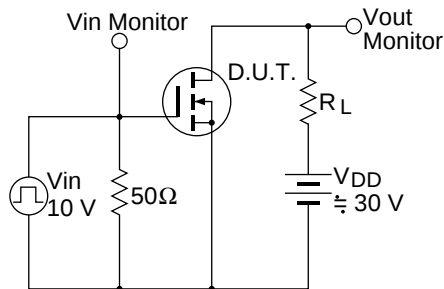
Avalanche Test Circuit



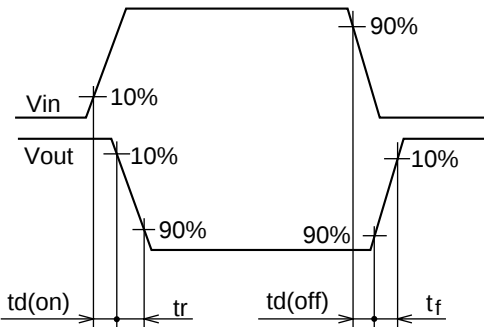
Avalanche Waveform



Switching Time Test Circuit



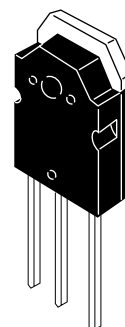
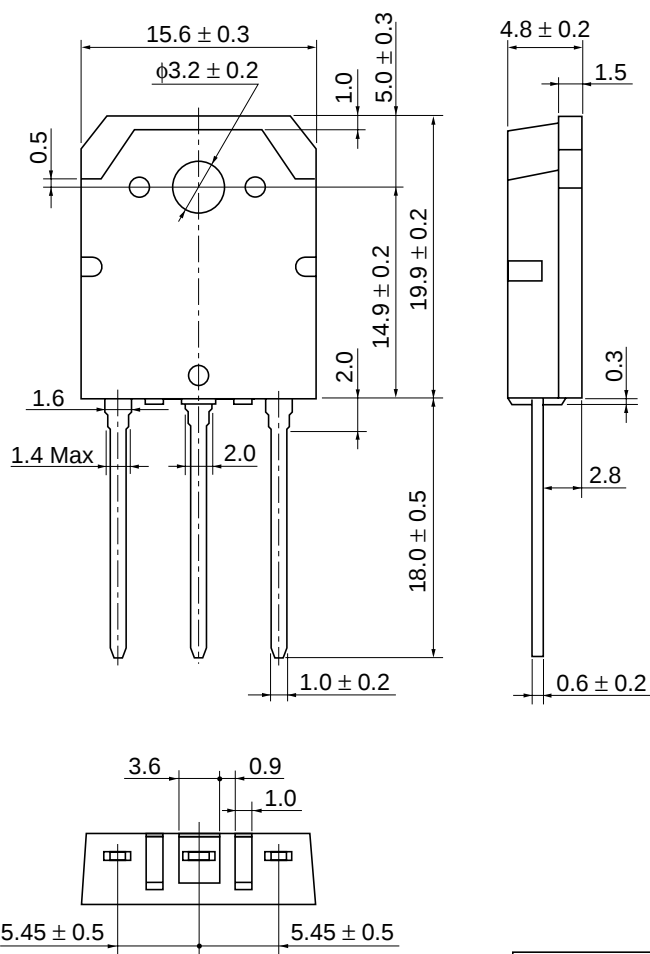
Switching Time Waveform



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	TO-3P
JEDEC	—
EIAJ	Conforms
Mass (reference value)	5.0 g

Cautions

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