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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2788

Silicon N Channel MOS FET High Speed Power Switching

RENESAS

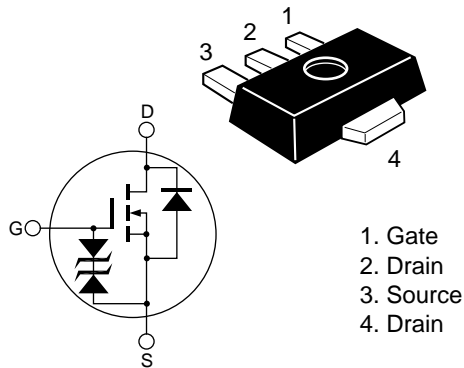
ADE-208-538 (Z)
1st. Edition
Jun 1997

Features

- Low on-resistance
 $R_{DS(on)} = 0.12\Omega$ typ ($V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$)
- Low drive current
- High speed switching
- 4V gate drive devices.

Outline

UPAK



Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	2	A
Drain peak current	$I_{D(pulse)}^{*1}$	4	A
Body to drain diode reverse drain current	I_{DR}	2	A
Channel dissipation	P_{ch}^{*2}	1	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$

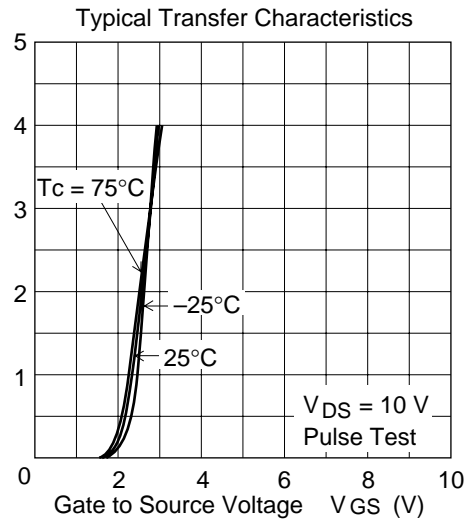
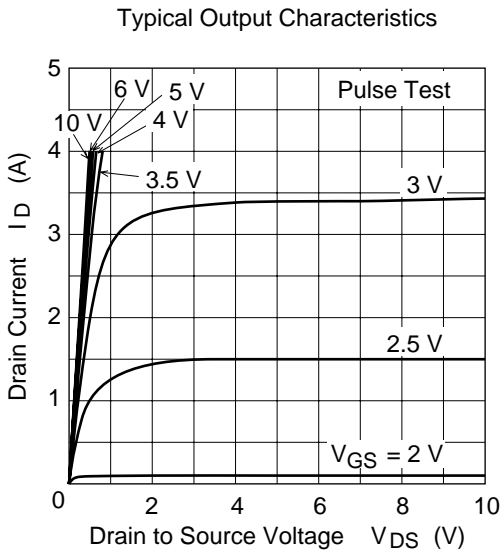
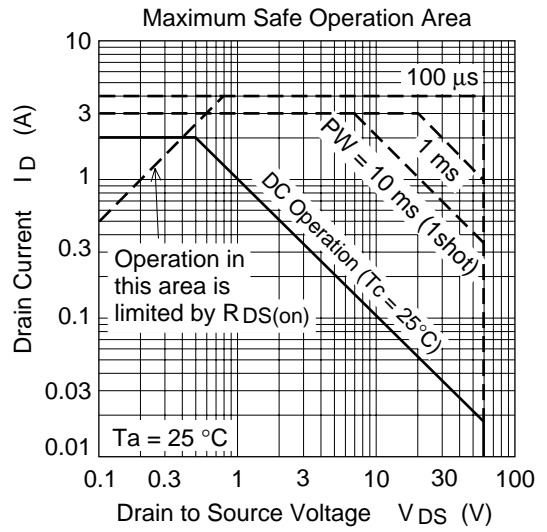
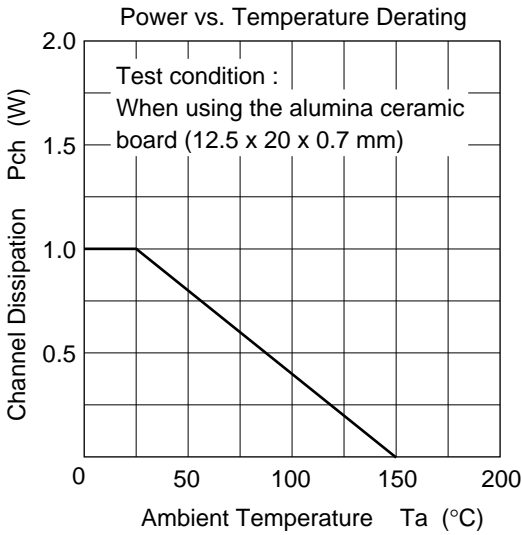
2. When using the alumina ceramic board (12.5 x 20 x 0.7 mm)

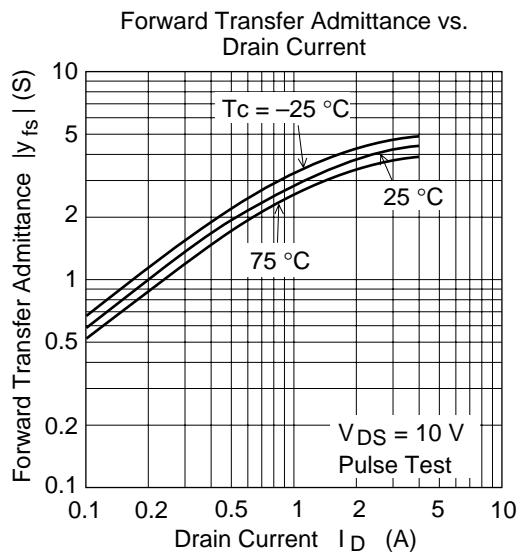
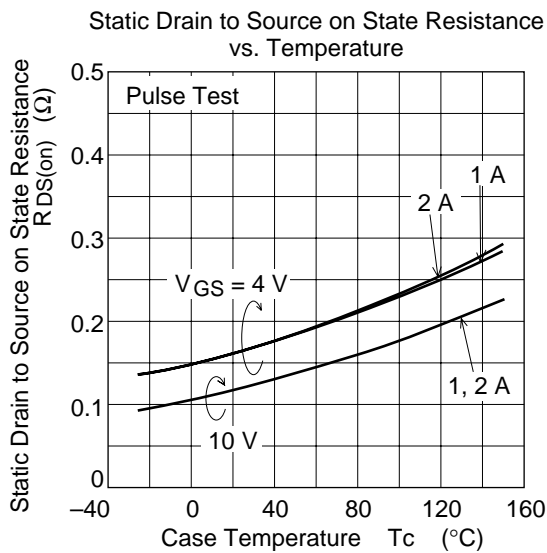
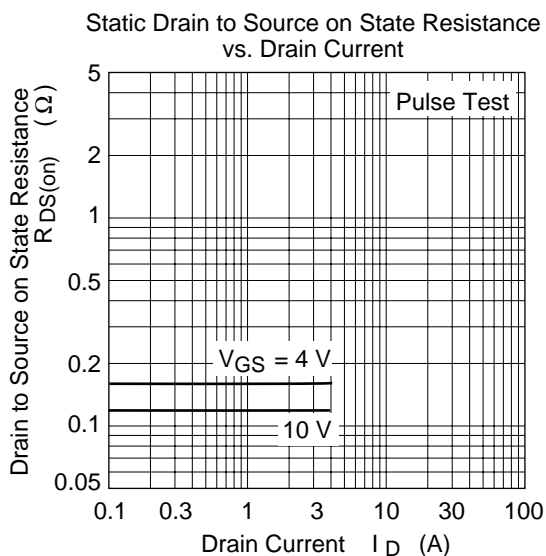
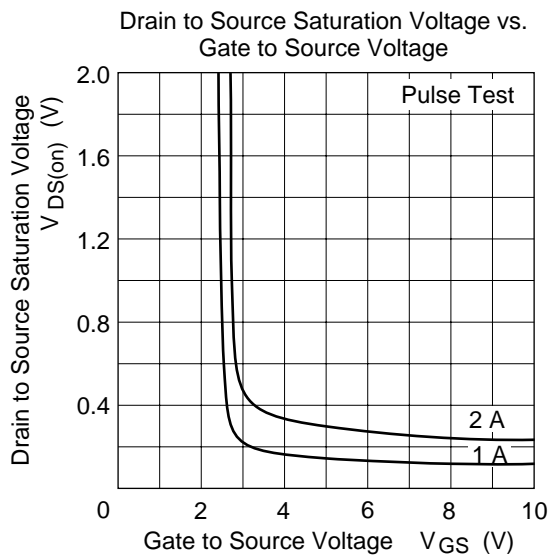
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1\text{mA}$, $V_{DS} = 10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	$I_D = 1\text{A}$, $V_{GS} = 10\text{V}^{*1}$
	$R_{DS(on)}$	—	0.16	0.25	Ω	$I_D = 1\text{A}$, $V_{GS} = 4\text{V}^{*1}$
Forward transfer admittance	$ y_{fs} $	1.6	2.8	—	S	$I_D = 1\text{A}$, $V_{DS} = 10\text{V}^{*1}$
Input capacitance	C_{iss}	—	180	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	C_{oss}	—	90	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	30	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	9	—	ns	$V_{GS} = 10\text{V}$, $I_D = 1\text{A}$
Rise time	t_r	—	15	—	ns	$R_L = 30\Omega$
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	
Fall time	t_f	—	35	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_D = 2\text{A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	35	—	ns	$I_F = 2\text{A}$, $V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

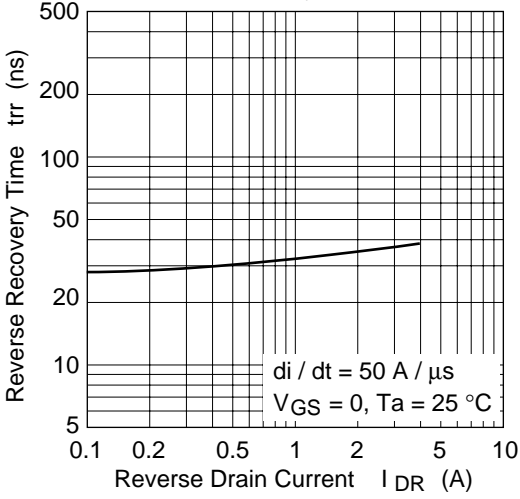
Notes: 1. Pulse test
2. Marking is "VY"

Main Characteristics

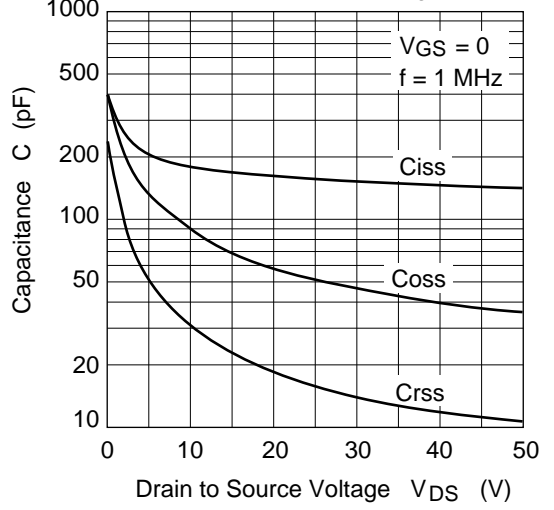




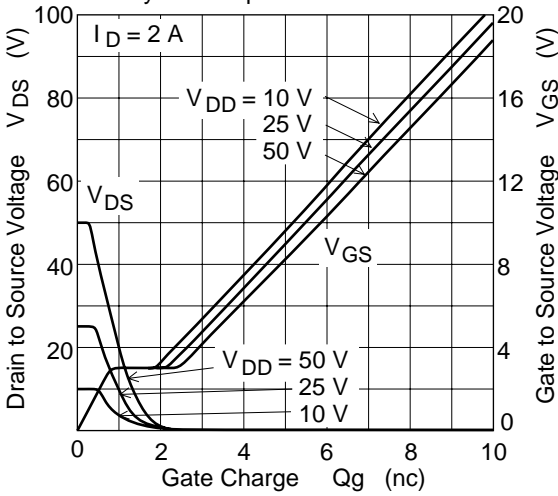
Body to Drain Diode Reverse Recovery Time



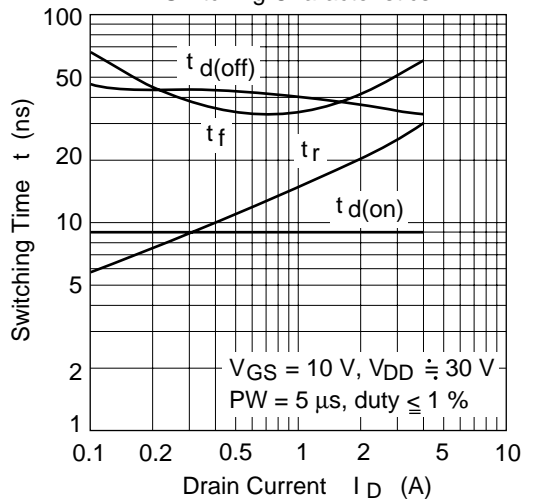
Typical Capacitance vs. Drain to Source Voltage

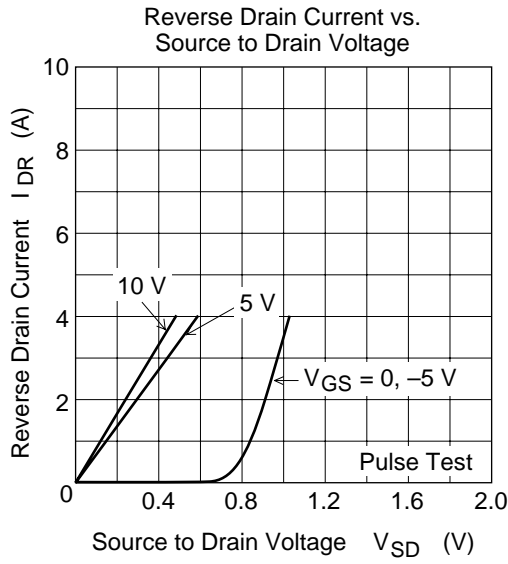


Dynamic Input Characteristics

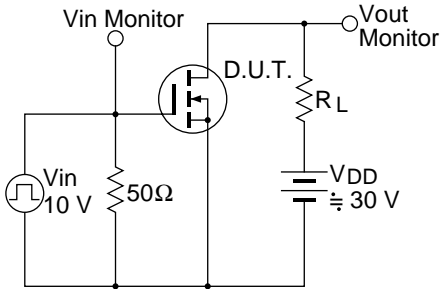


Switching Characteristics

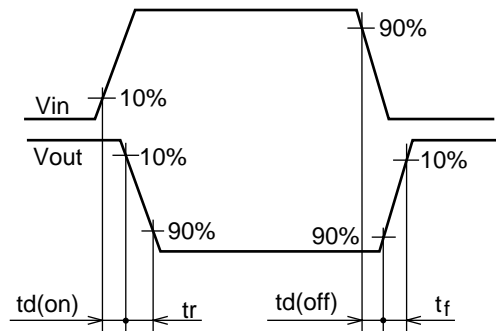




Switching Time Test Circuit



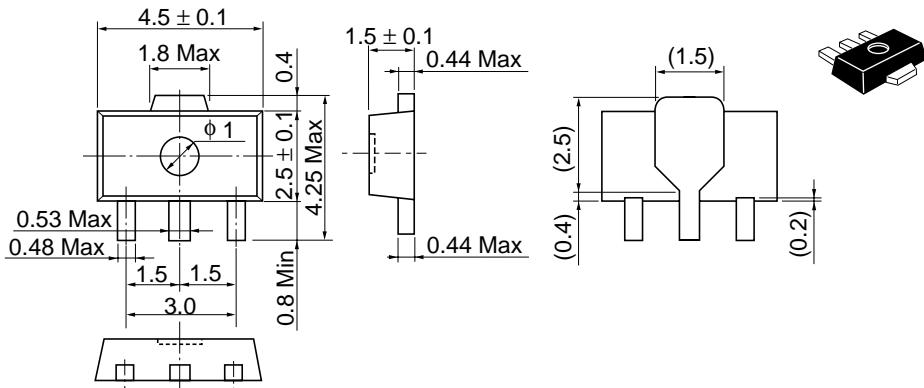
Waveform



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.050 g

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