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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2796(L), 2SK2796(S)

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

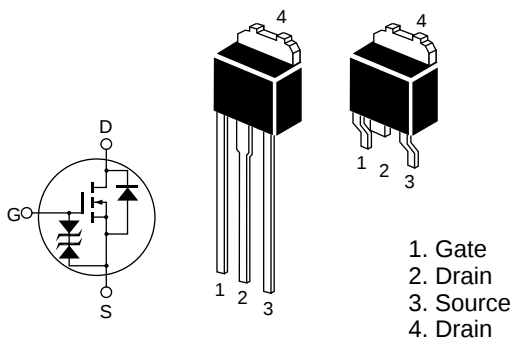
ADE-208-534C (Z)
4th. Edition
Jul. 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.12\Omega$ typ.
- 4V gate drive devices.
- High speed switching

Outline

DPAK | 1



2SK2796(L), 2SK2796(S)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	5	A
Drain peak current	I _{D(pulse)} ^{Note1}	20	A
Body-drain diode reverse drain current	I _{DR}	5	A
Avalanche current	I _{AP} ^{Note3}	5	A
Avalanche energy	E _{AR} ^{Note3}	2.14	mJ
Channel dissipation	Pch ^{Note2}	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg 50 Ω

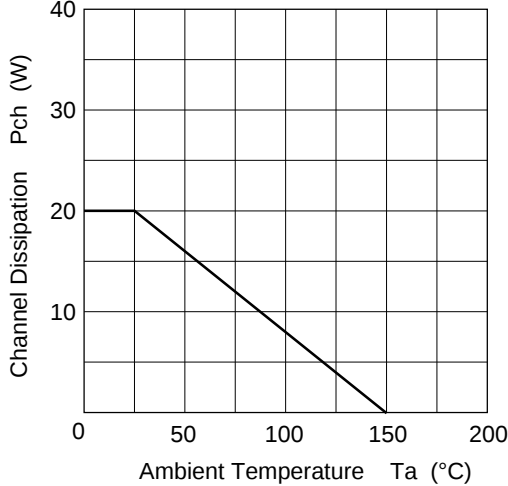
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1\text{mA}$, $V_{DS} = 10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	$I_D = 3\text{A}$, $V_{GS} = 10\text{V}$ ^{Note4}
Static drain to source on state resistance	$R_{DS(on)}$	—	0.16	0.25	Ω	$I_D = 3\text{A}$, $V_{GS} = 4\text{V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	2.5	4.0	—	S	$I_D = 3\text{A}$, $V_{DS} = 10\text{V}$ ^{Note4}
Input capacitance	C_{iss}	—	180	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	C_{oss}	—	90	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	30	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	9	—	ns	$V_{GS} = 10\text{V}$, $I_D = 3\text{A}$
Rise time	t_r	—	25	—	ns	$R_L = 10\Omega$
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	55	—	ns	
Body-drain diode forward voltage	V_{DF}	—	1.0	—	V	$I_F = 5\text{A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 5\text{A}$, $V_{GS} = 0$ $diF/dt = 50\text{A}/\mu\text{s}$

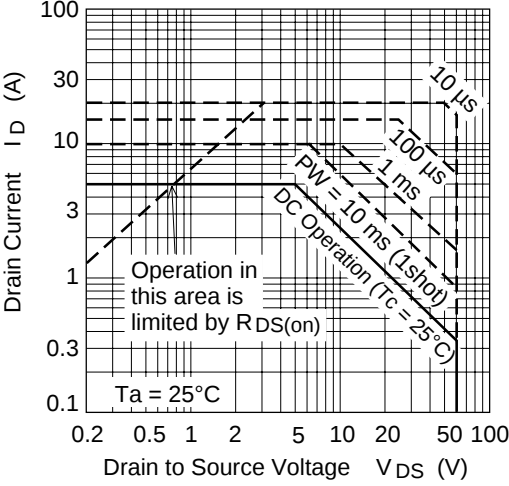
Note: 4. Pulse test

Main Characteristics

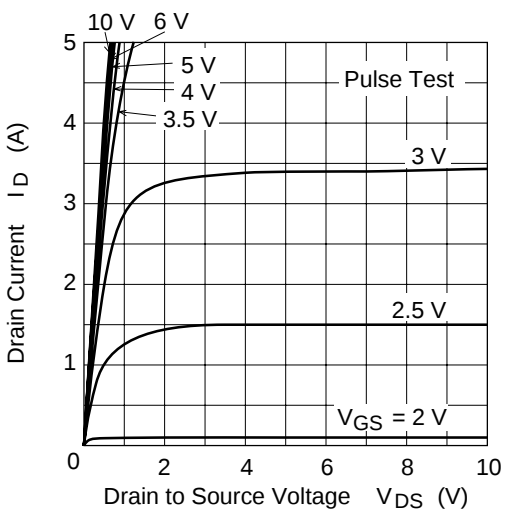
Power vs. Temperature Derating



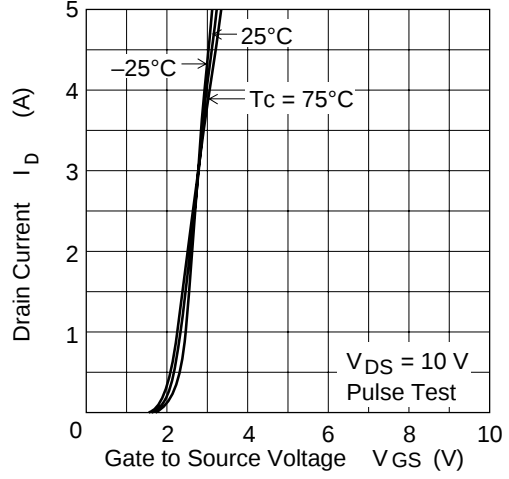
Maximum Safe Operation Area



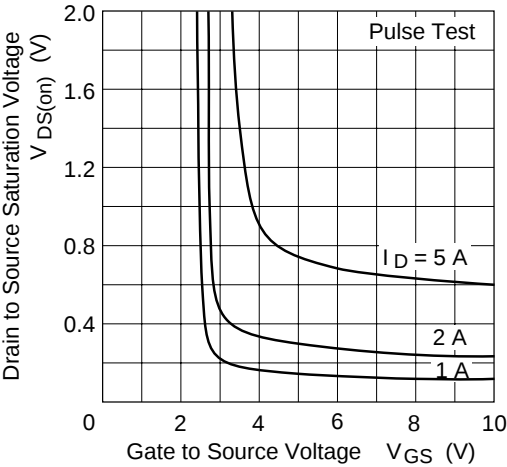
Typical Output Characteristics



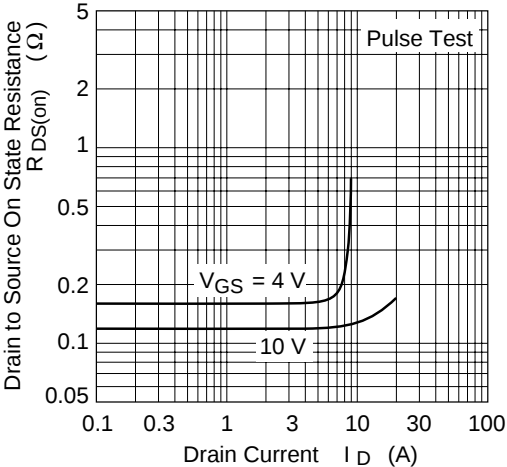
Typical Transfer Characteristics



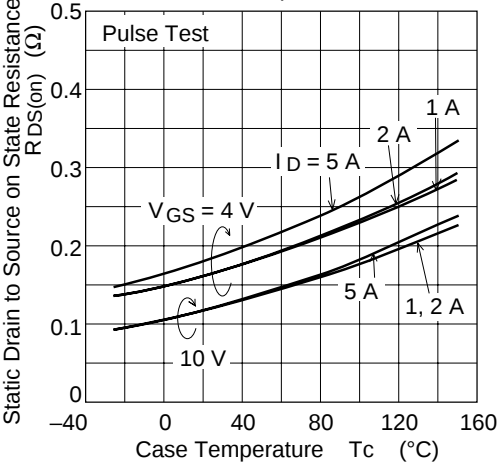
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



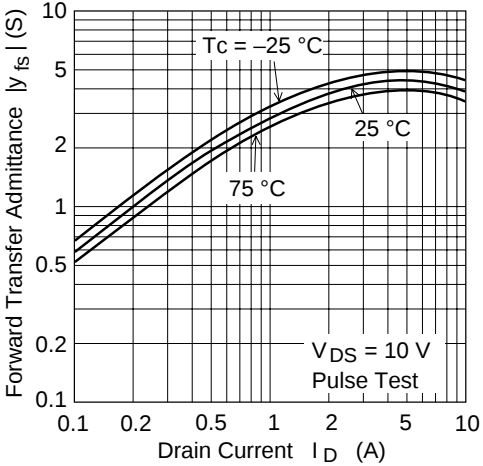
Static Drain to Source on State Resistance
vs. Drain Current

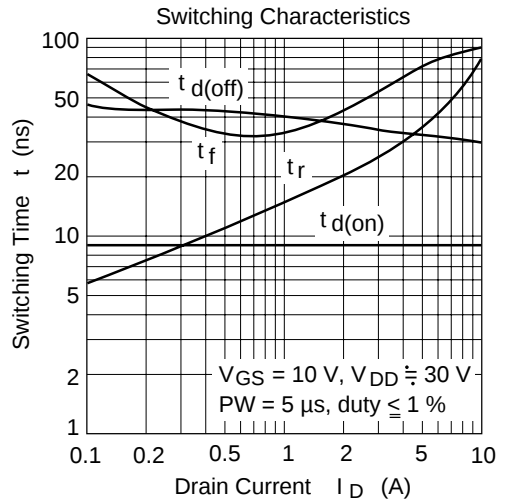
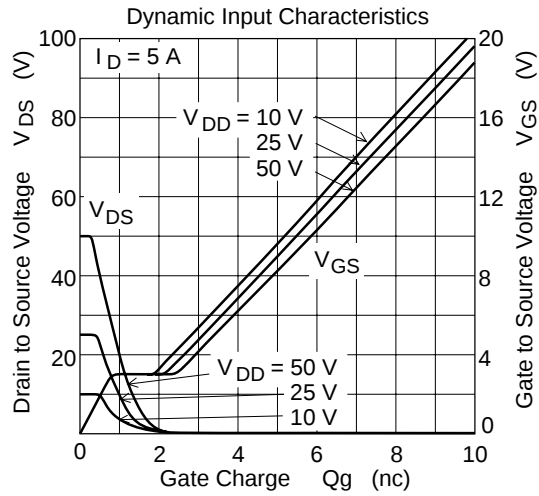
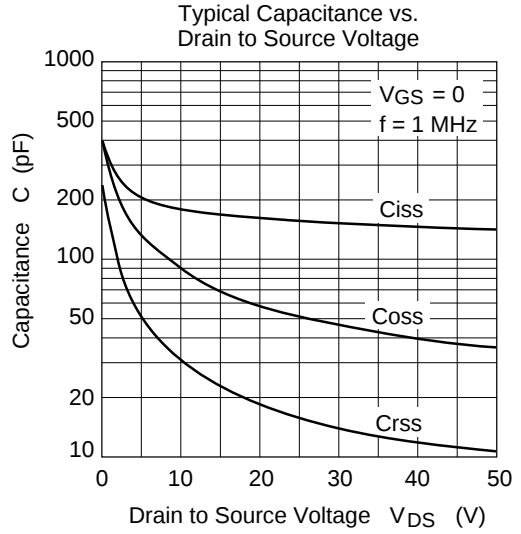
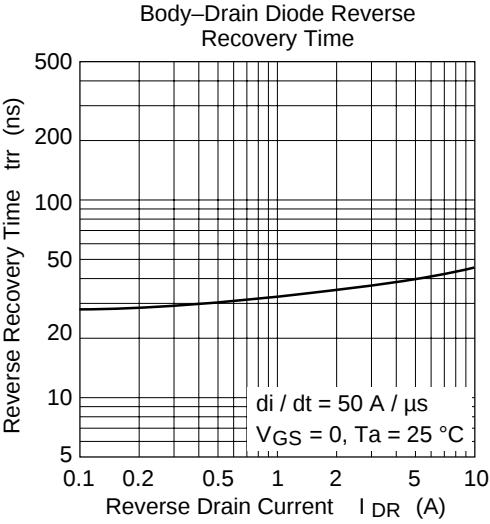


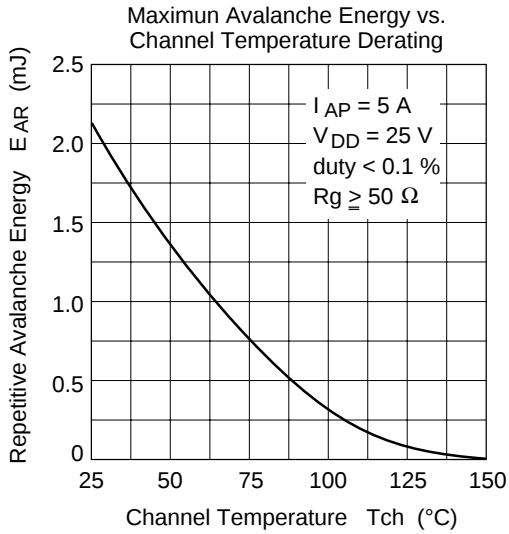
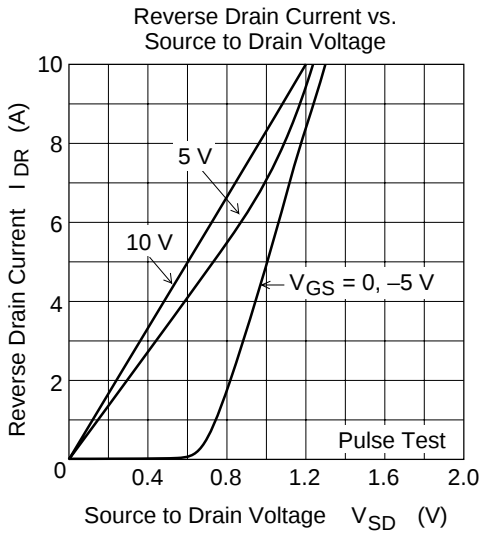
Static Drain to Source on State Resistance
vs. Temperature



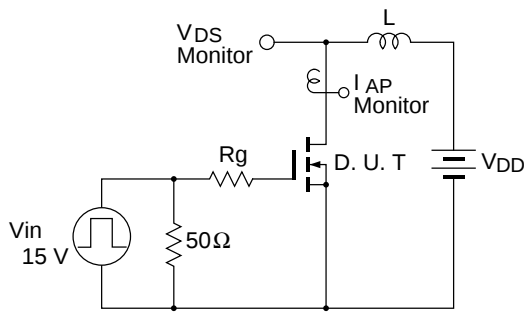
Forward Transfer Admittance vs.
Drain Current





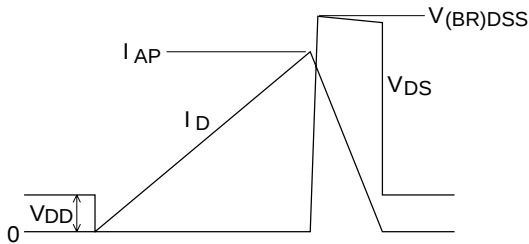


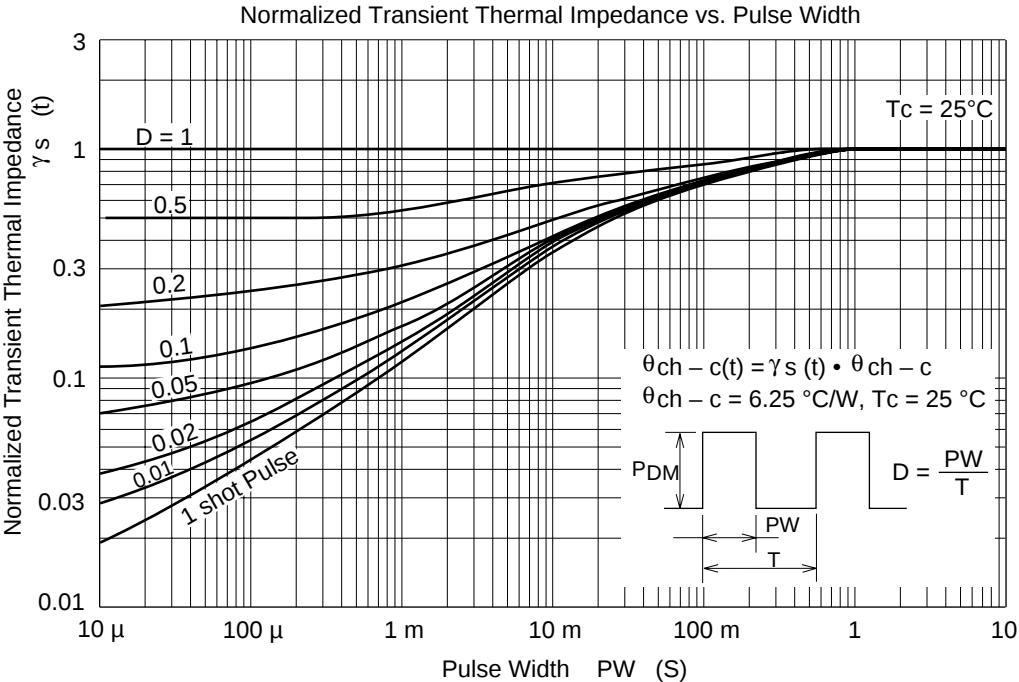
Avalanche Test Circuit



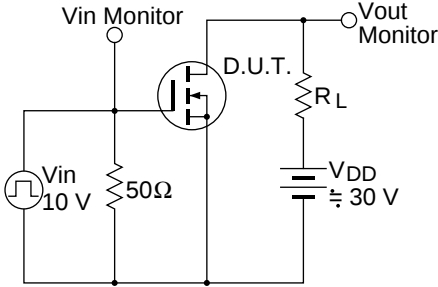
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

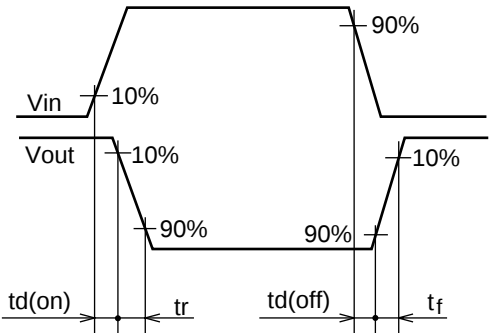




Switching Time Test Circuit

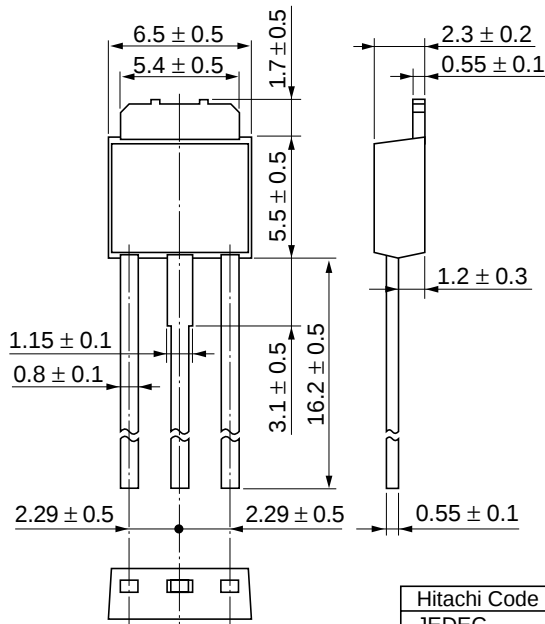


Waveform



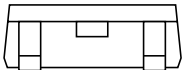
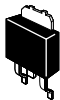
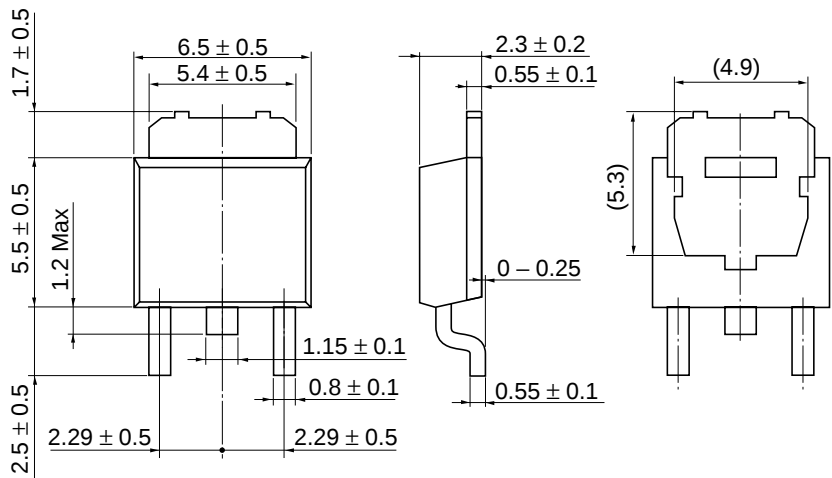
Package Dimensions

As of January, 2001
Unit: mm



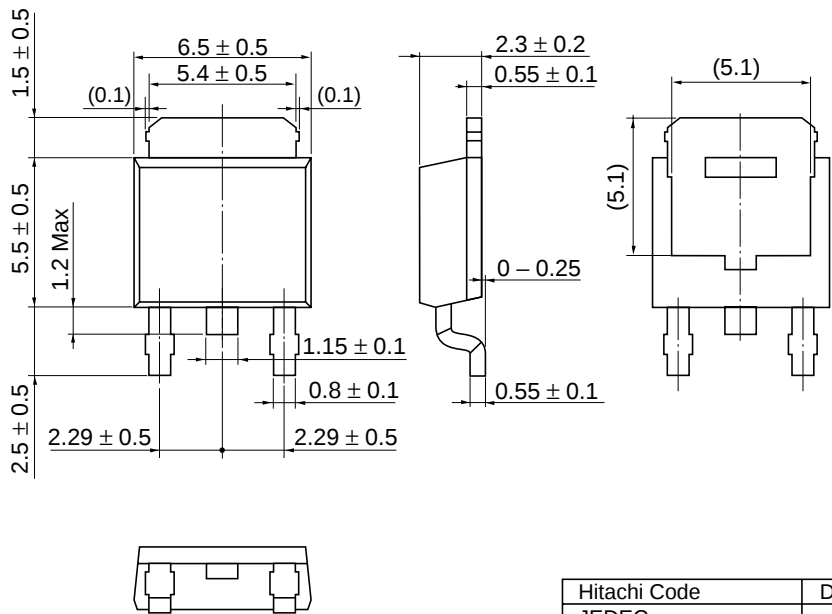
Hitachi Code	DPAK (L)-(1)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.42 g

As of January, 2001
Unit: mm



Hitachi Code	DPAK (S)-(1),(2)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

As of January, 2001
Unit: mm



Hitachi Code	DPAK (S)-(3)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

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