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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2925(L),2SK2925(S)

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

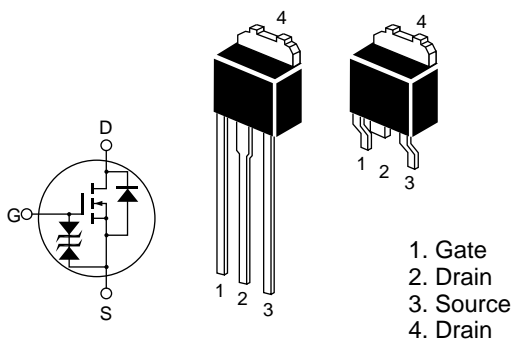
ADE-208-549C (Z)
4th. Edition
Jul. 1998

Features

- Low on-resistance
 $R_{DS} = 0.060 \Omega$ typ.
- High speed switching
- 4V gate drive device can be driven from 5V source

Outline

DPAK-2



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	40	A
Body-drain diode reverse drain current	I_{DR}	10	A
Avalanche current	I_{AP} ^{Note3}	10	A
Avalanche energy	E_{AR} ^{Note3}	8.5	mJ
Channel dissipation	Pch ^{Note2}	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

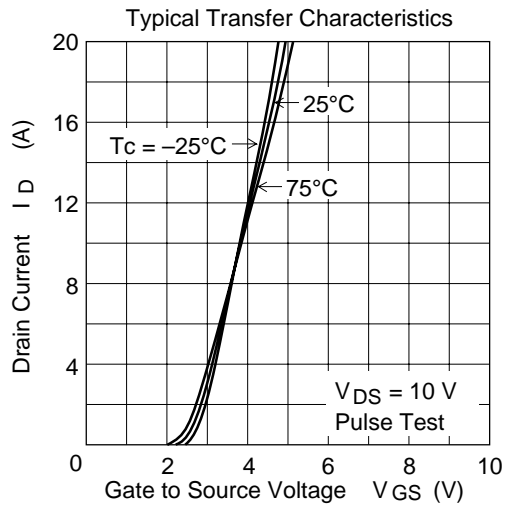
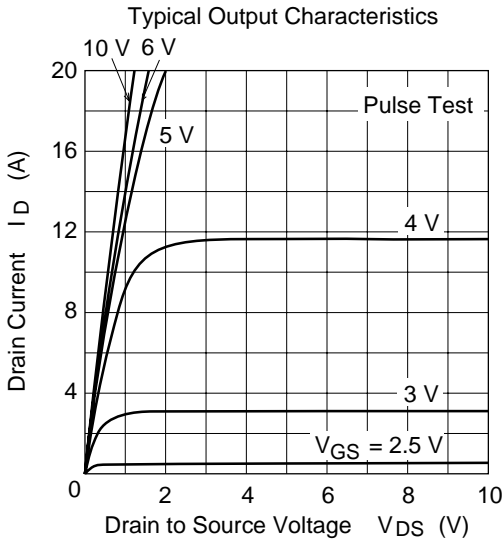
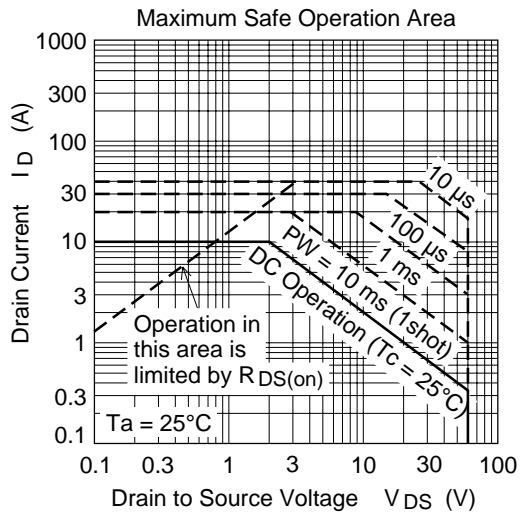
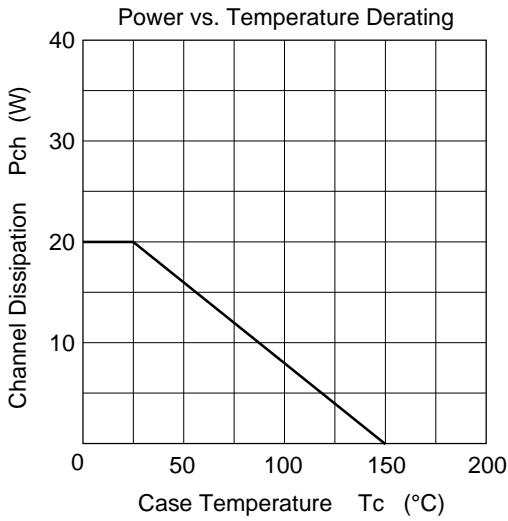
Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ C$
3. Value at $Tch = 25^\circ C$, $R_g = 50\Omega$

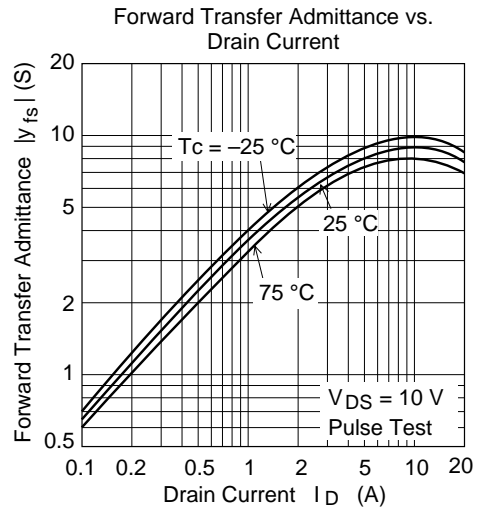
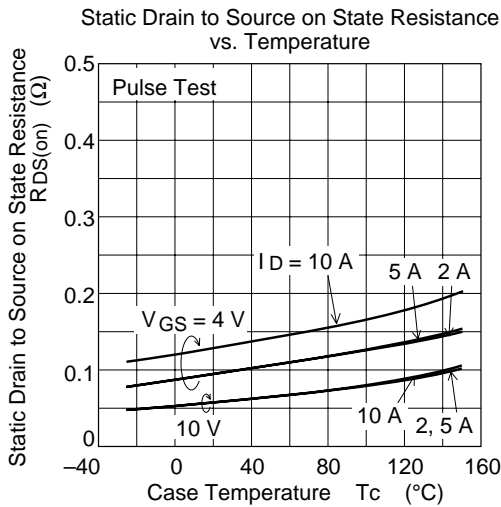
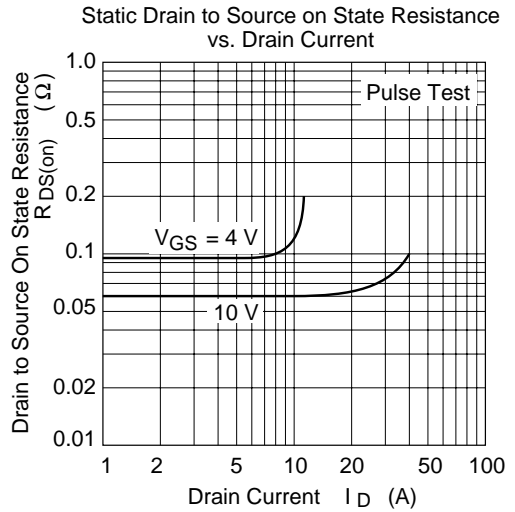
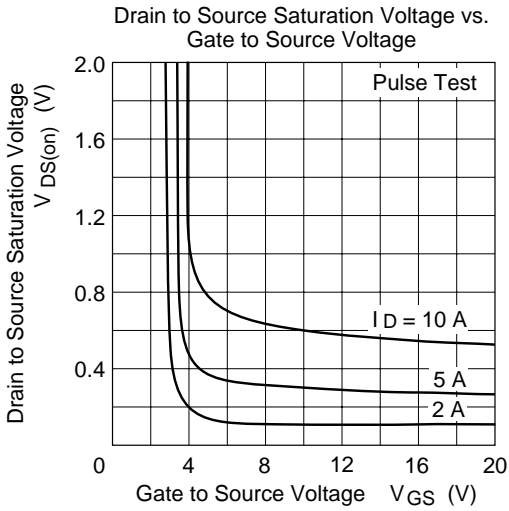
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10\text{mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60\text{V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1\text{mA}, V_{DS} = 10\text{V}$
Static drain to source on state	$R_{DS(on)}$	—	0.060	0.080	Ω	$I_D = 5\text{A}, V_{GS} = 10\text{V}$ ^{Note4}
resistance	$R_{DS(on)}$	—	0.095	0.160	Ω	$I_D = 5\text{A}, V_{GS} = 4\text{V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	5	8	—	S	$I_D = 5\text{A}, V_{DS} = 10\text{V}$ ^{Note4}
Input capacitance	Ciss	—	350	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	Coss	—	190	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	70	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$I_D = 5\text{A}, V_{GS} = 10\text{V}$
Rise time	t_r	—	55	—	ns	$R_L = 6\Omega$
Turn-off delay time	$t_{d(off)}$	—	60	—	ns	
Fall time	t_f	—	70	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_F = 10\text{A}, V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = 10\text{A}, V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

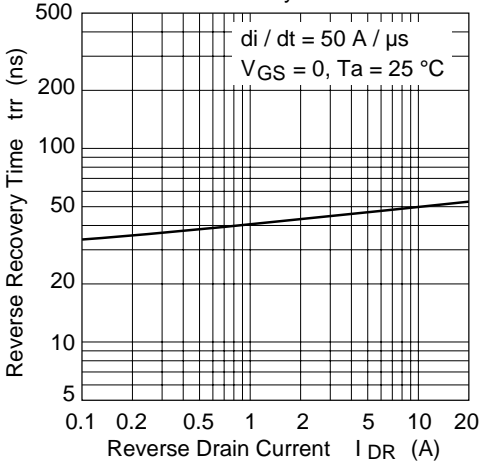
Note: 4. Pulse test

Main Characteristics

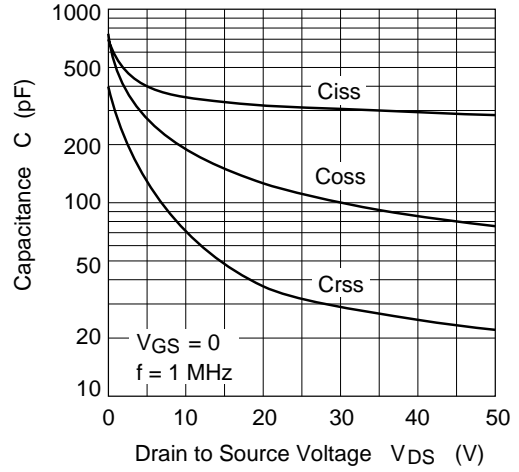




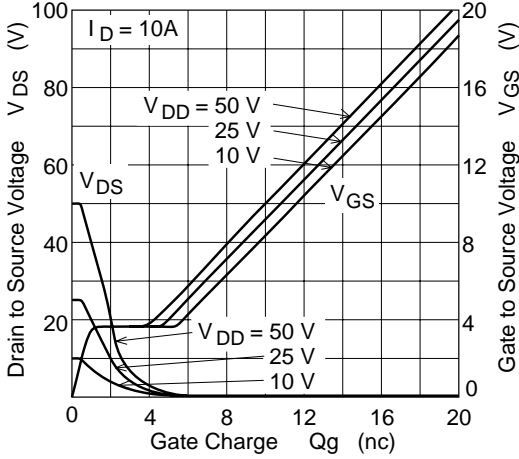
Body-Drain Diode Reverse Recovery Time



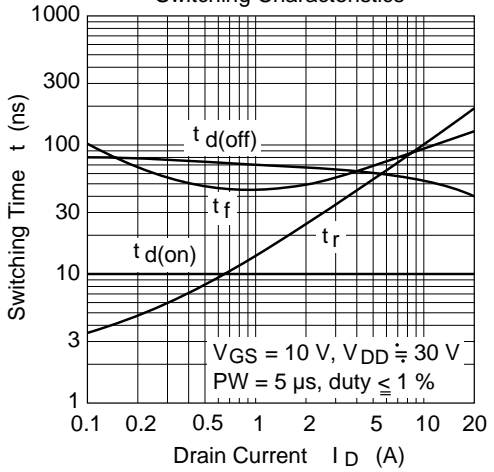
Typical Capacitance vs. Drain to Source Voltage

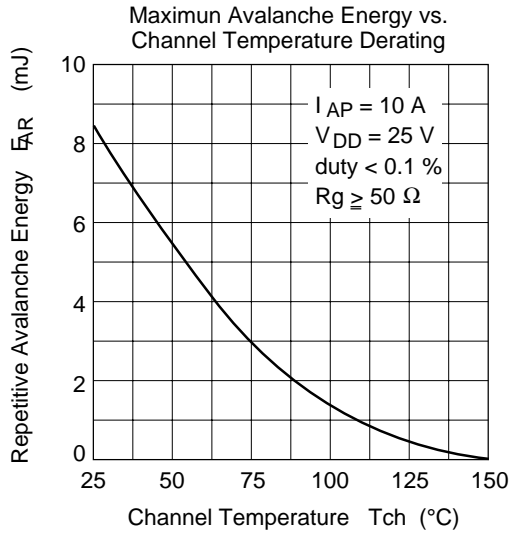
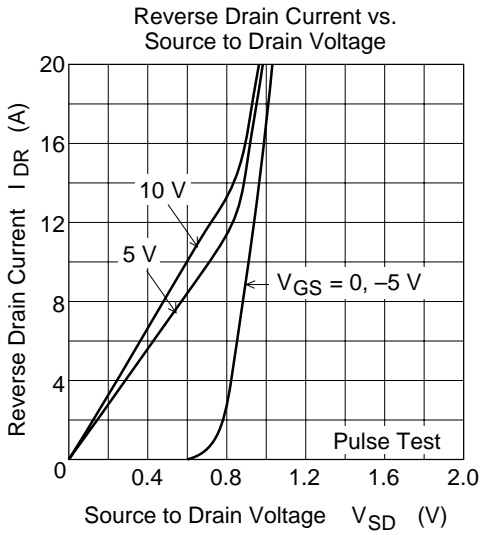


Dynamic Input Characteristics

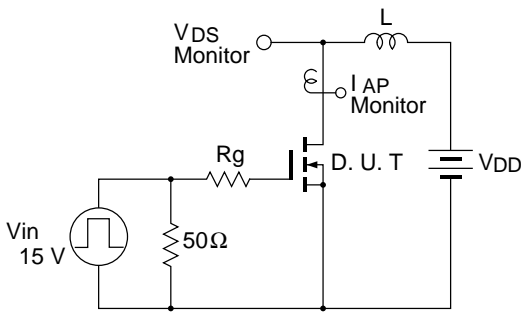


Switching Characteristics



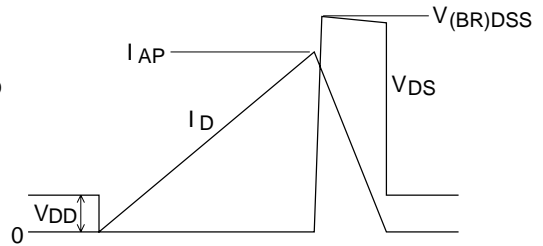


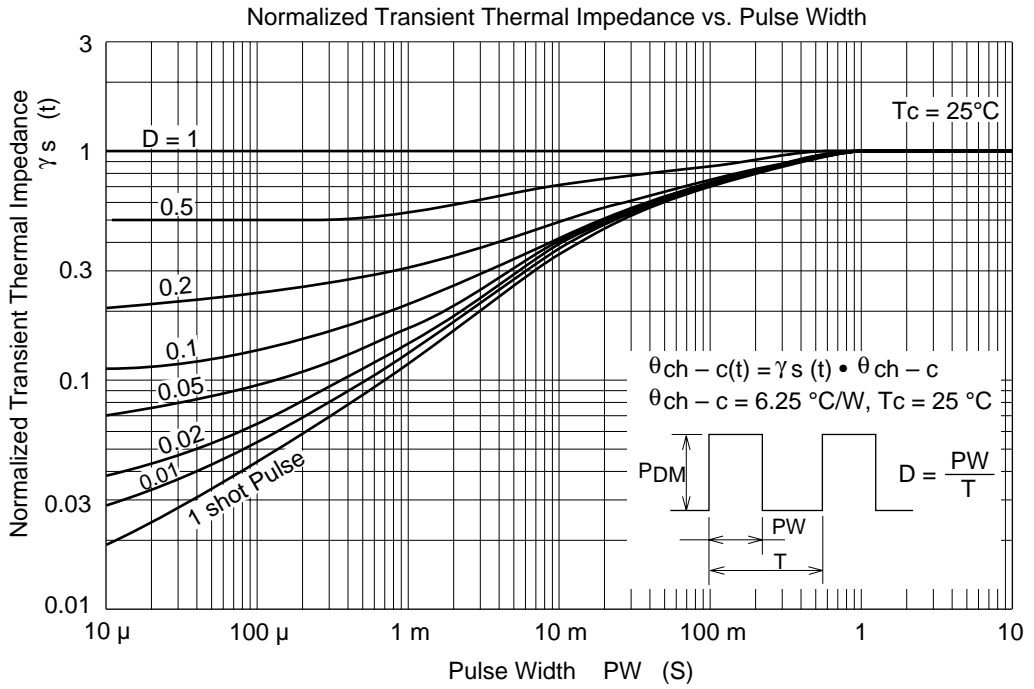
Avalanche Test Circuit



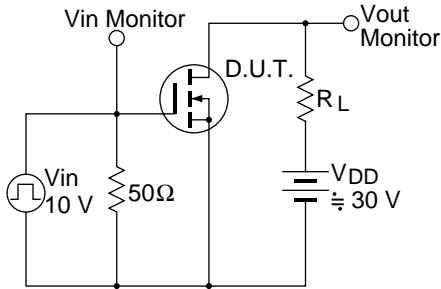
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

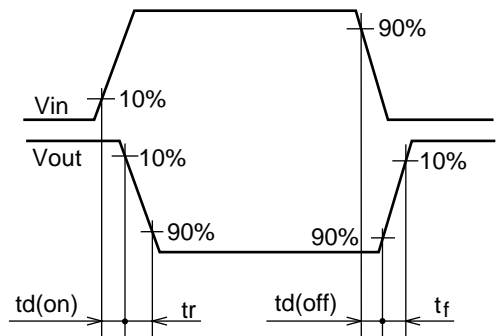




Switching Time Test Circuit

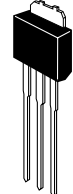
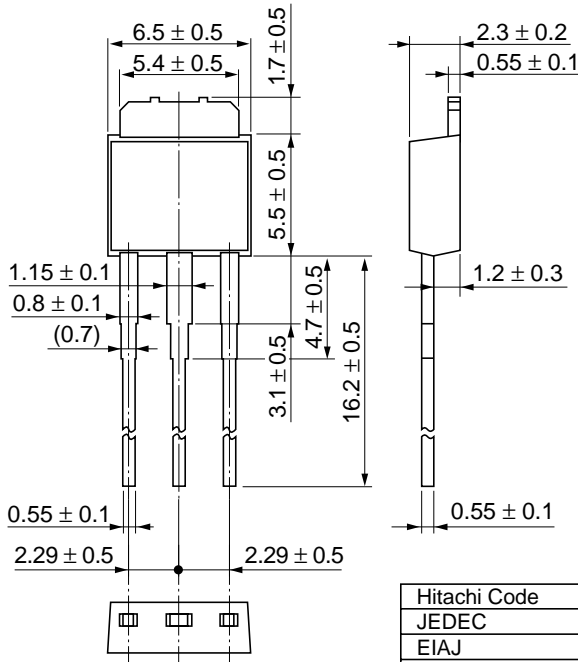


Waveform



Package Dimensions

As of January, 2001
Unit: mm

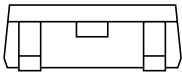
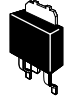
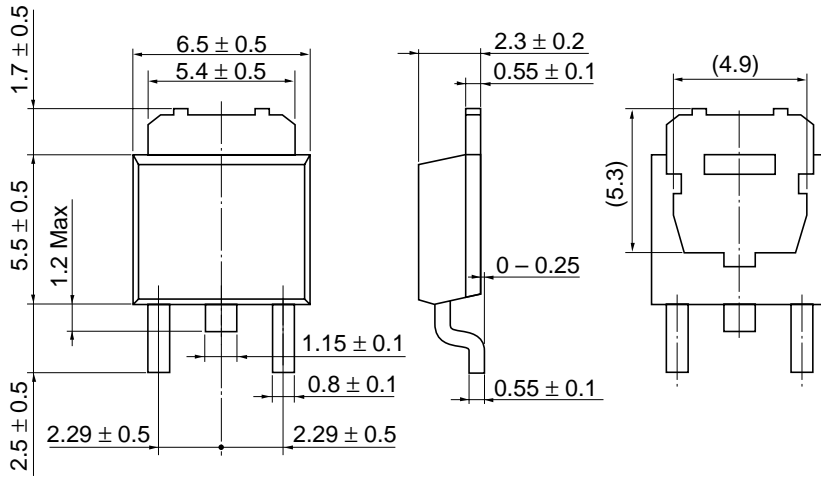


Hitachi Code	DPAK (L)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	0.42 g

2SK2925(L),2SK2925(S)

As of January, 2001

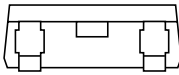
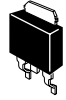
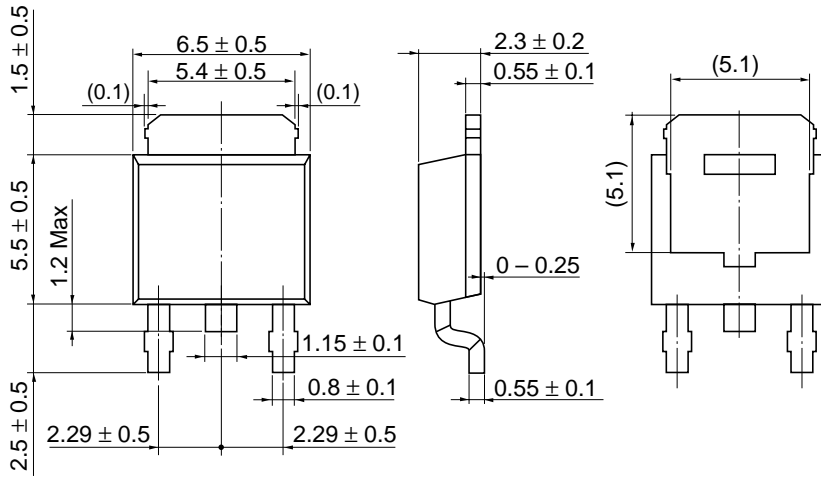
Unit: mm



Hitachi Code	DPAK (S)-(1),(2)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

As of January, 2001

Unit: mm



Hitachi Code	DPAK (S)-(3)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

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