To all our customers

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Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2980

Silicon N Channel MOS FET
High Speed Power Switching

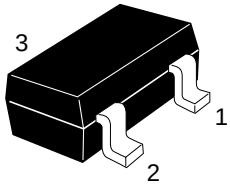
ADE-208-571B (Z)
3rd. Edition
Jul. 1998

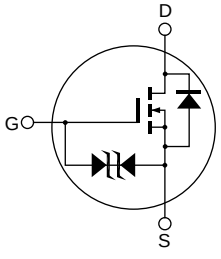
Features

- Low on-resistance
  $R_{DS(on)}$ = 0. 2Ω typ. (V_{GS} = 4 V, I_D = 500 mA)
- 2.5V gate drive devices.
- Small package (MPAK)

Outline

MPAK





1. Source
2. Gate
3. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	+12	V
		–10	V
Drain current	I_D	1.0	A
Drain peak current	$I_{D(pulse)}$ Note1	4	A
Channel dissipation	Pch Note2	0.8	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

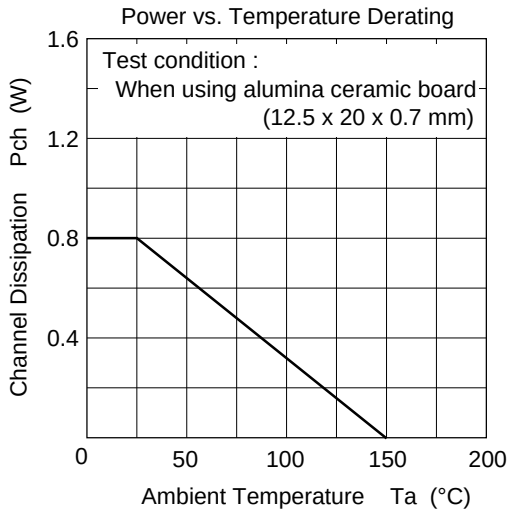
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. Value at when using alumina ceramic board (12.5 x 20 x 0.7 mm)

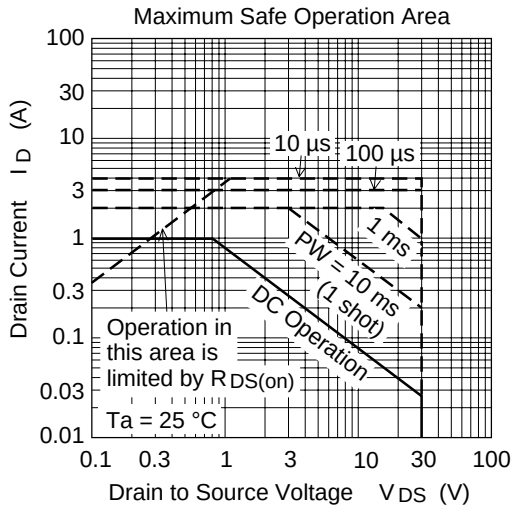
Electrical Characteristics (Ta = 25°C)

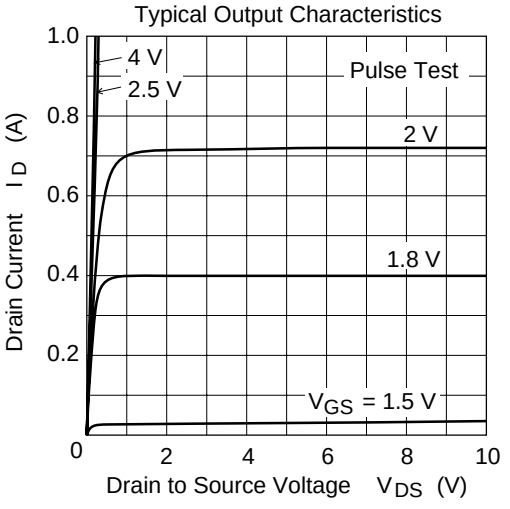
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 100µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	+12	—	—	V	I_G = +100µA, V_{DS} = 0
		–10	—	—	V	I_G = –100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	1.0	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±5.0	µA	V_{GS} = ±8V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	I_D = 10µA, V_{DS} = 5V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.2	0.28	Ω	I_D = 500 mA V_{GS} = 4V [Note3]
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.5	Ω	I_D = 500 mA V_{GS} = 2.5V [Note3]
Forward transfer admittance	$\|y_{fs}\|$	1.2	2.0	—	S	I_D = 500 mA V_{DS} = 10V [Note3]
Input capacitance	Ciss	—	155	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	75	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	35	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	V_{GS} = 4V, I_D = 500 mA
Rise time	t_r	—	30	—	ns	R_L = 20Ω
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	30	—	ns	

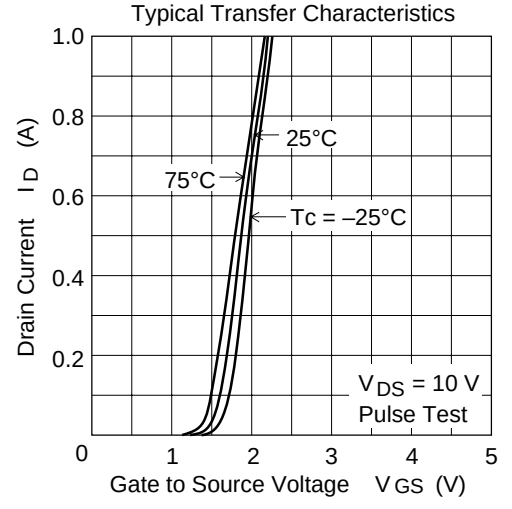
Note: 3. Pulse test
4. Marking is “ZZ– ”

Main Characteristics

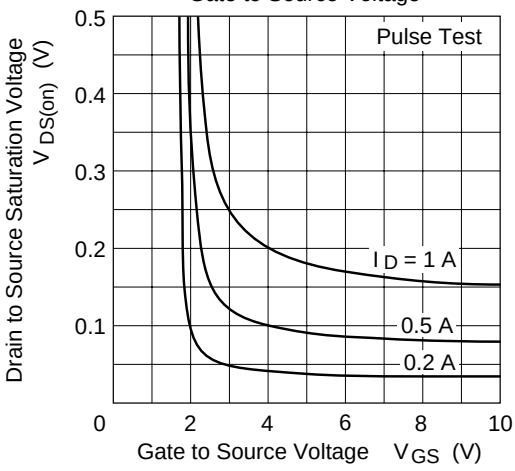




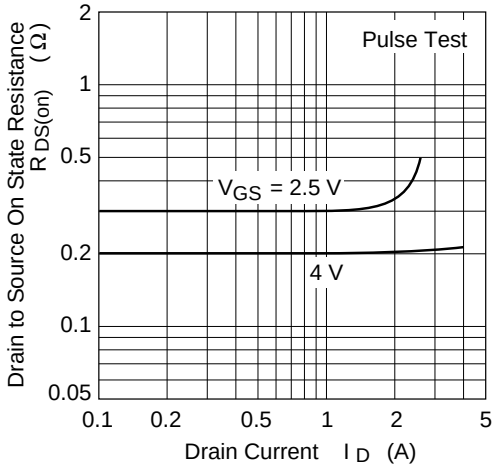




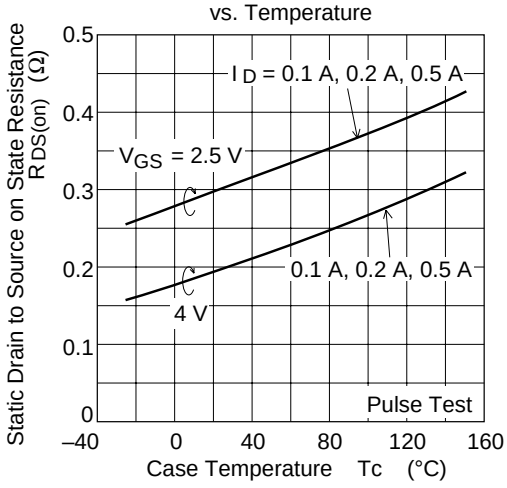
Drain to Source Saturation Voltage vs. Gate to Source Voltage



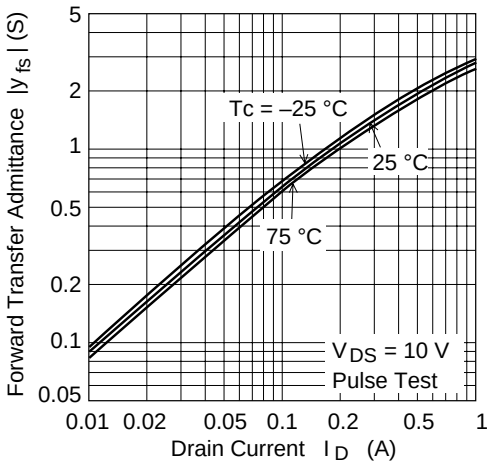
Static Drain to Source on State Resistance vs. Drain Current



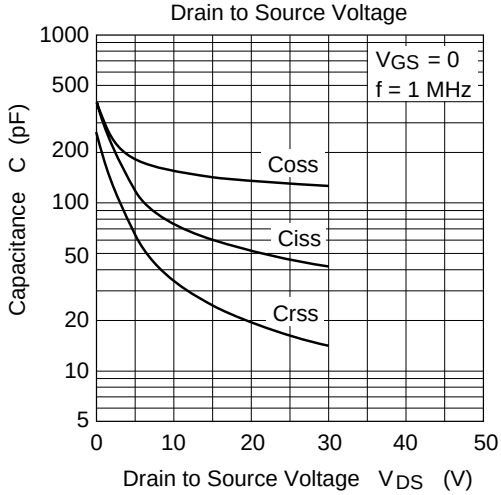
Static Drain to Source on State Resistance vs. Temperature



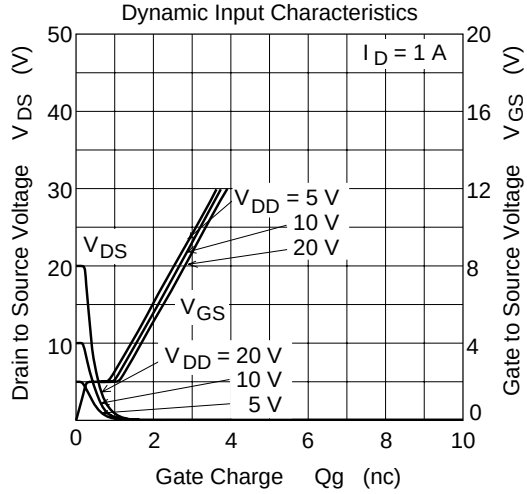
Forward Transfer Admittance vs. Drain Current



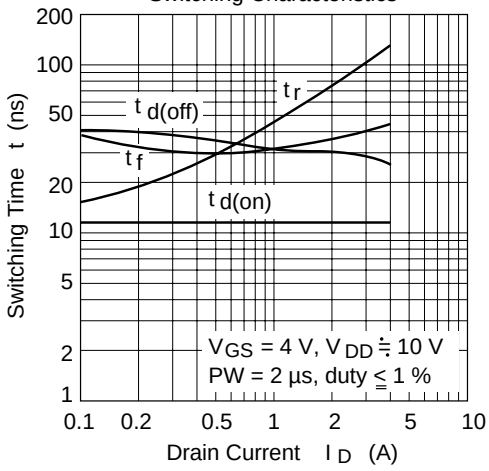
Typical Capacitance vs.
Drain to Source Voltage



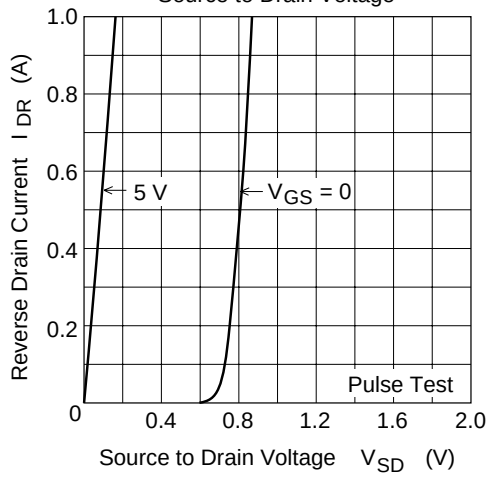
Dynamic Input Characteristics



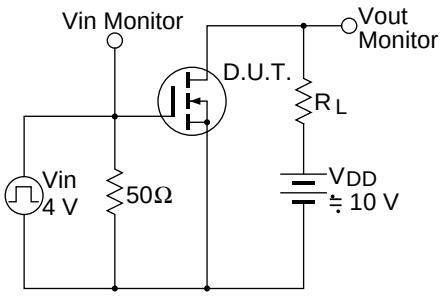
Switching Characteristics



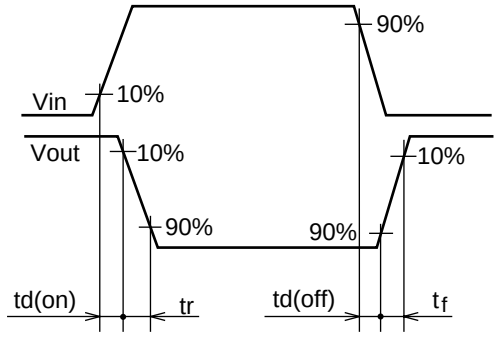
Reverse Drain Current vs.
Source to Drain Voltage



Switching Time Test Circuit



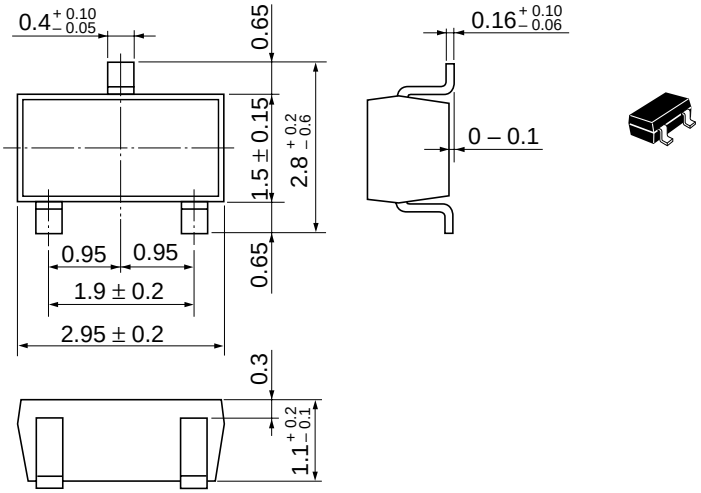
Waveform



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	MPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.011 g

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