

To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK3274(L), 2SK3274(S)

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

ADE-208-960 (Z)

1st. Edition

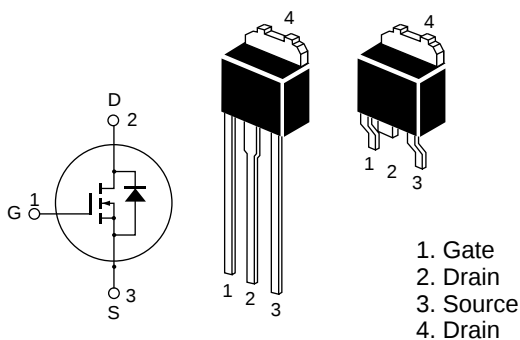
Mar. 2001

Features

- Low on-resistance
- $R_{DS(on)} = 10\text{ m}\Omega$ typ.
- 4.5 V gate drive device
- High speed switching

External View

DPAK-2



Absolute Maximum Ratings (Ta = 25°C)

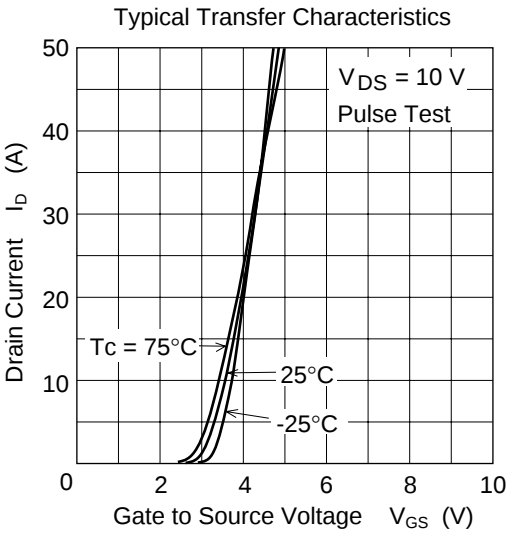
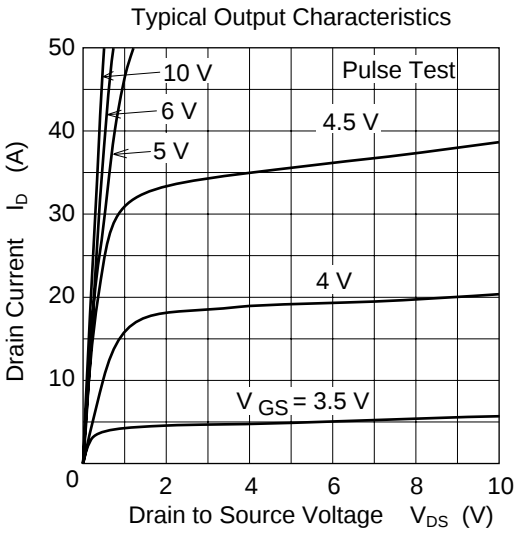
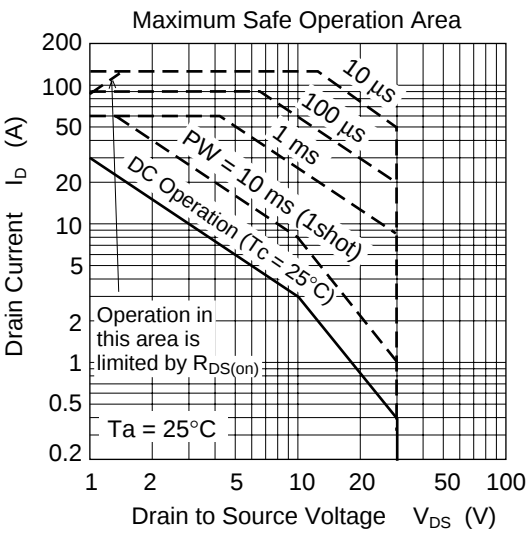
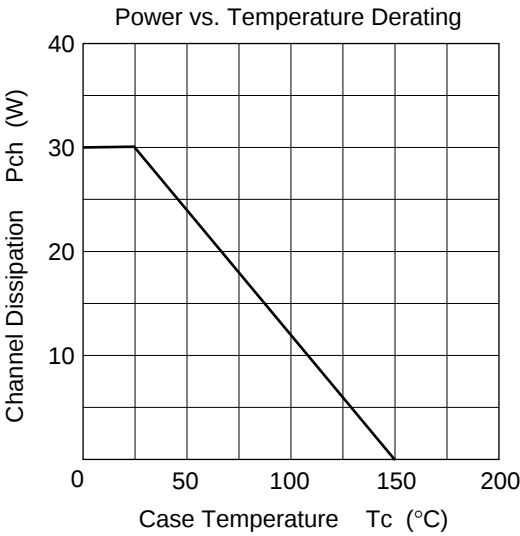
Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	30	A
Drain peak current	I_D (pulse)* ¹	120	A
Body-drain diode reverse drain current	I_{DR}	30	A
Avalanche current	I_{AP} * ³	20	A
Avalanche energy	E_{AR} * ³	40	mJ
Channel dissipation	P_{ch} * ²	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

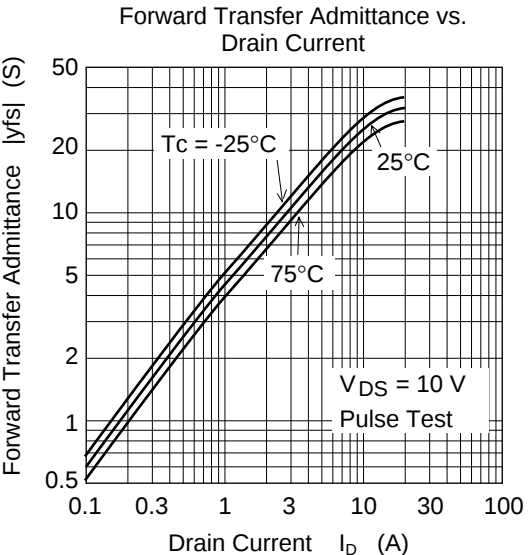
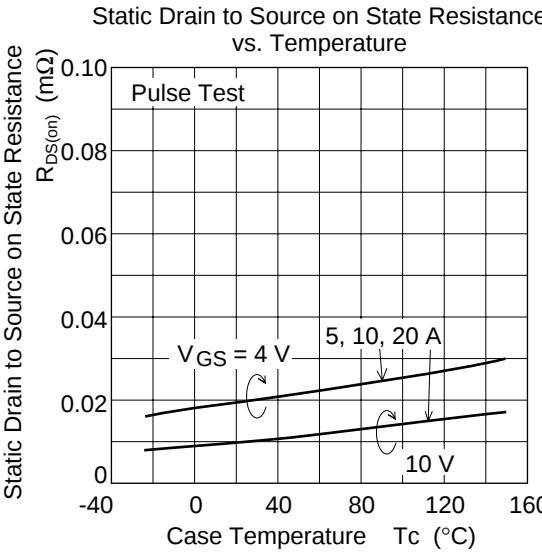
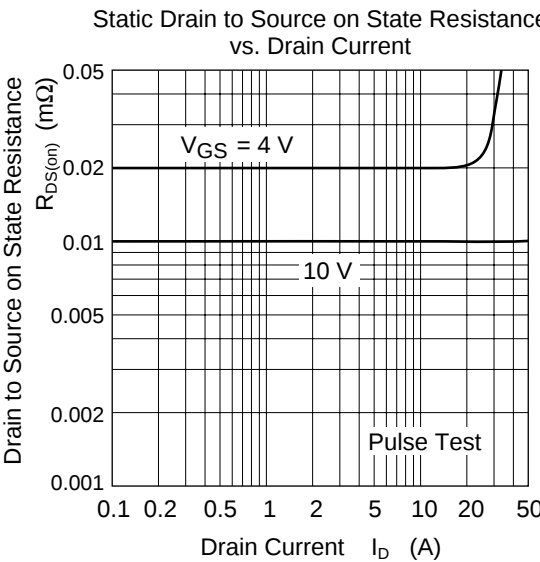
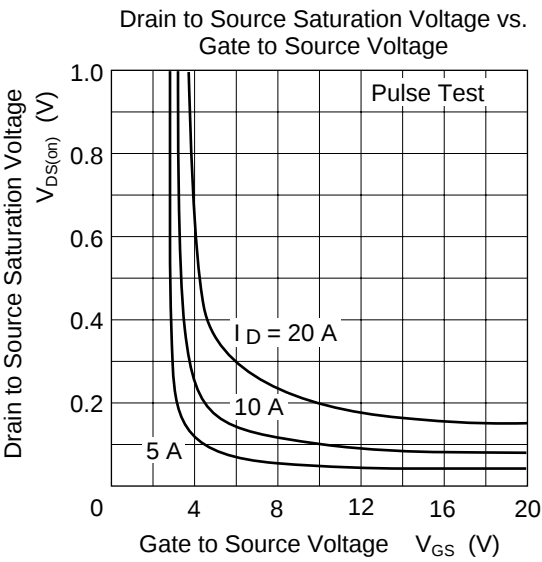
Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. Value at Tc = 25°C
3. Value at Tch = 25°C: $R_g \geq 50 \Omega$

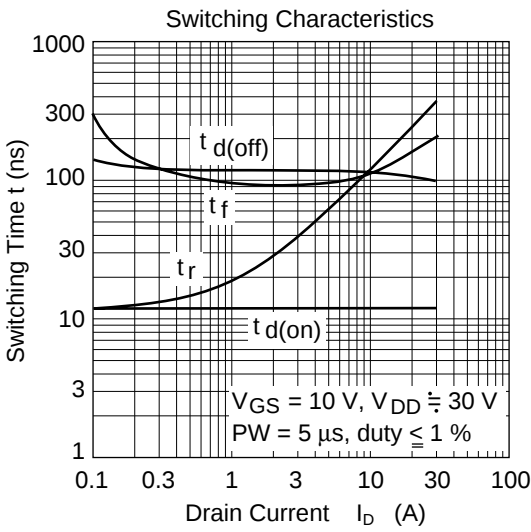
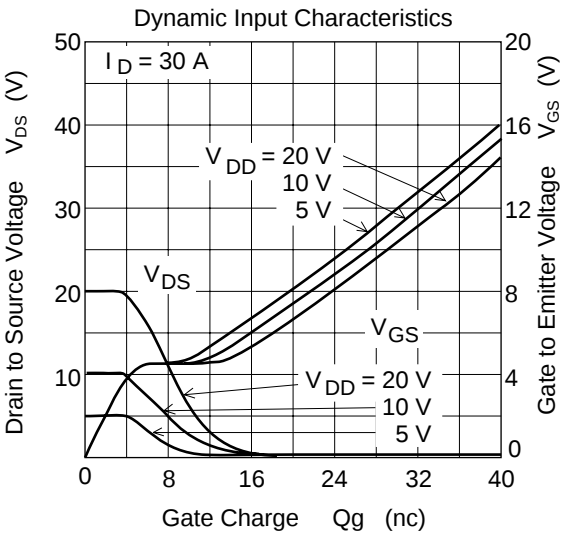
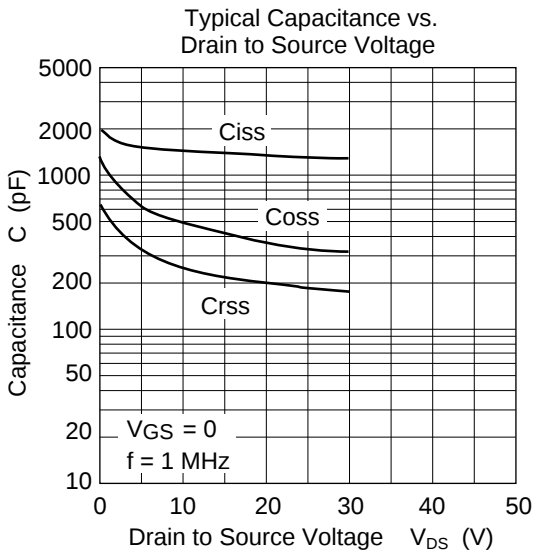
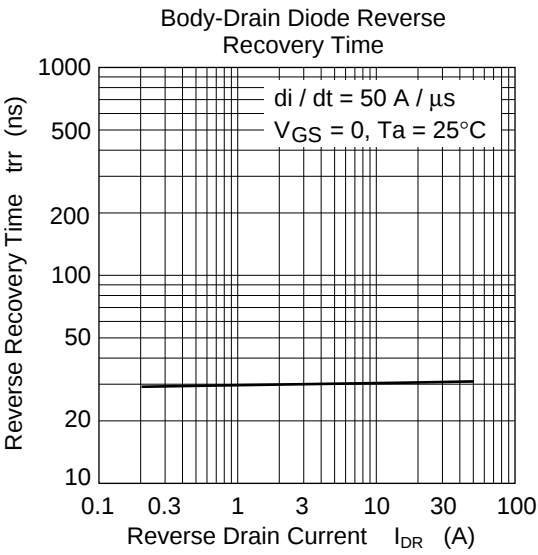
Electrical Characteristics (Ta = 25°C)

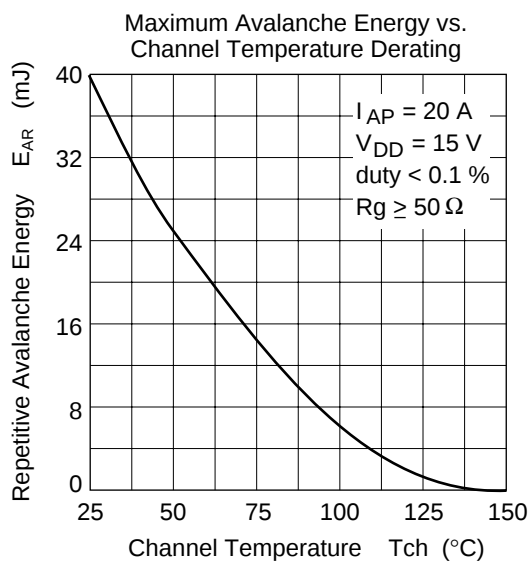
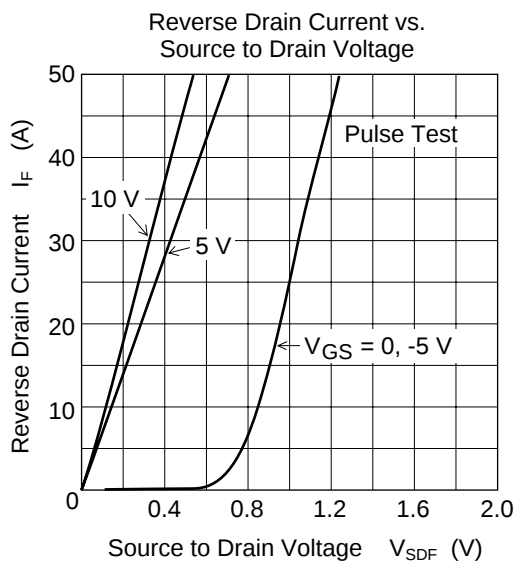
Item	Symbol	Min	Typ	Max	Unijt	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	3.0	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}^{*1}$
Forward transfer admittance	$ y_{fs} $	18	30	—	S	$I_D = 15 \text{ A}$, $V_{DS} = 10 \text{ V}^{*1}$
Static drain to source on state resistance	$R_{DS(on)}$	—	10	13	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}^{*1}$
	$R_{DS(on)}$	—	20	30	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 4.5 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	1500	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	500	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	250	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	27	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	6	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	5	—	nc	$I_D = 30 \text{ A}$
Turn-on delay time	$t_d(on)$	—	22	—	ns	$V_{GS} = 10 \text{ V}$
Rise time	t_r	—	170	—	ns	$I_D = 15 \text{ A}$
Turn-off delay time	$t_d(off)$	—	110	—	ns	$R_L = 2 \Omega$
Fall time	t_f	—	145	—	ns	
Body-drain diode forward voltage	V_{DF}	—	1.0	—	V	$I_F = 30 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	35	—	ns	$I_F = 30 \text{ A}$, $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Note: 1. Pulse test

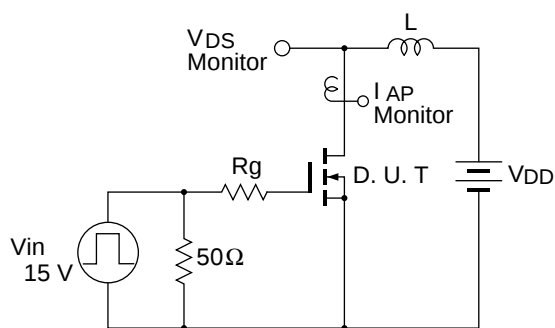






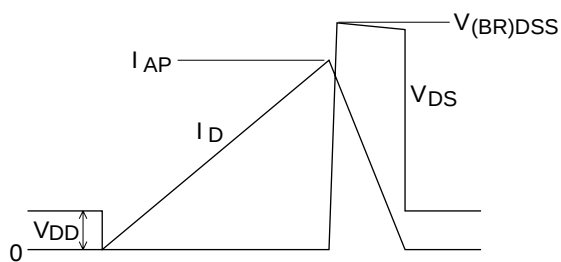


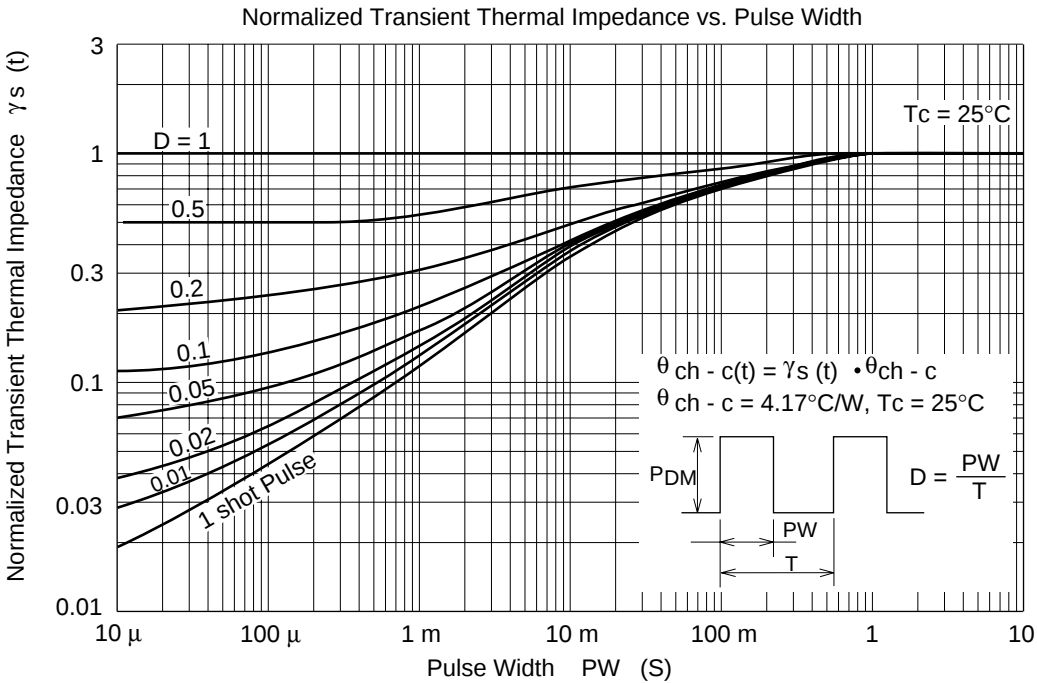
Avalanche Test Circuit



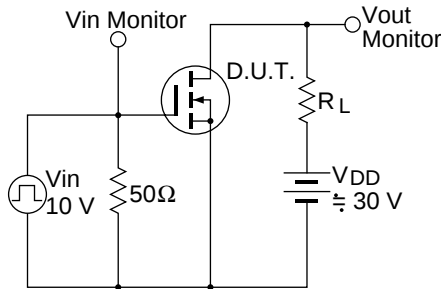
Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

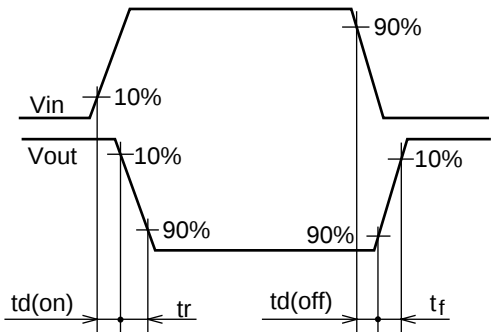




Switching Time Test Circuit

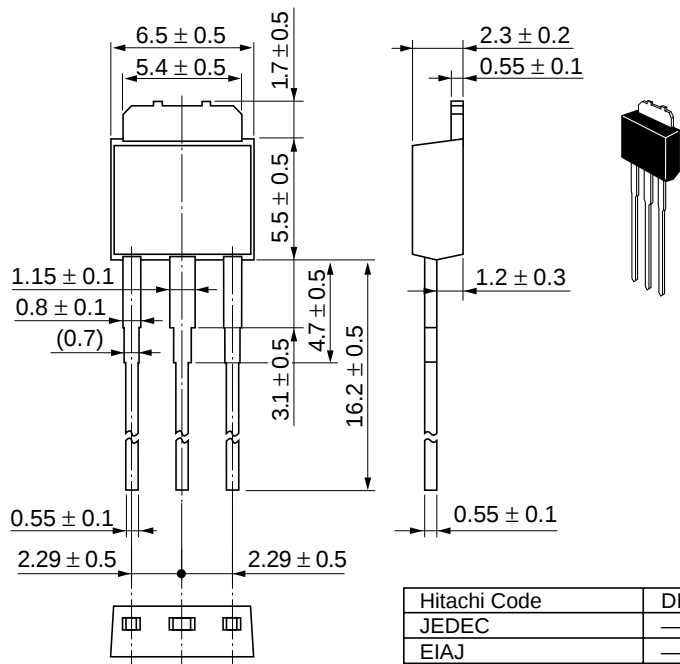


Waveform



Package Dimensions

As of January, 2001
Unit: mm

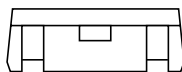
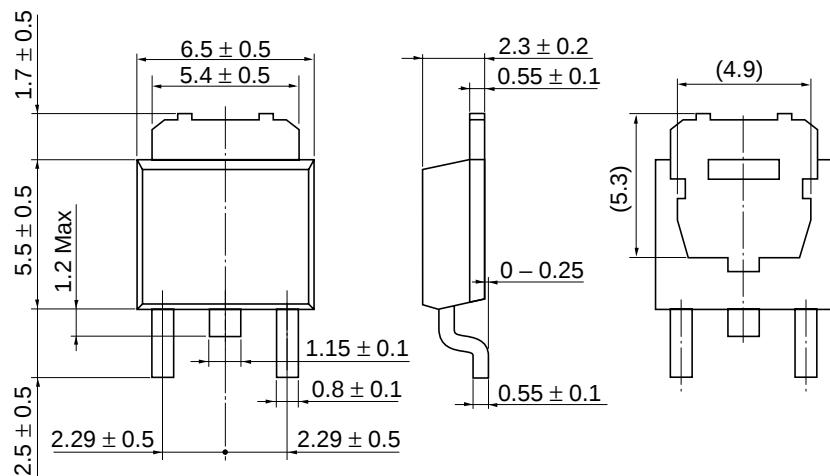


Hitachi Code	DPAK (L)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	0.42 g

2SK3274(L), 2SK3274(S)

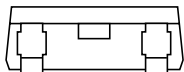
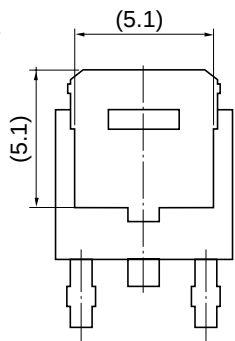
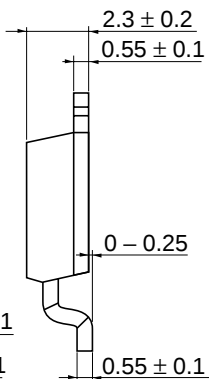
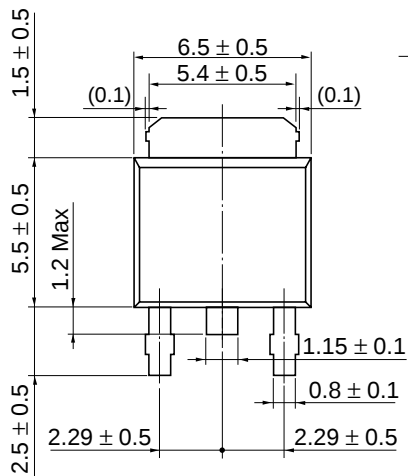
As of January, 2001

Unit: mm



Hitachi Code	DPAK (S)-(1),(2)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

As of January, 2001
Unit: mm



Hitachi Code	DPAK (S)-(3)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

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