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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

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2SK3348

Silicon N Channel MOS FET High Speed Switching

RENESAS

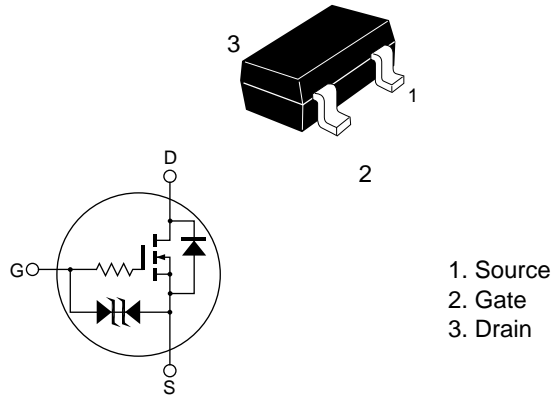
ADE-208-772 A (Z)
2nd.Edition.
June 1999

Features

- Low on-resistance
 $R_{DS} = 1.6 \Omega$ typ. ($V_{GS} = 4 \text{ V}$, $I_D = 50 \text{ mA}$)
 $R_{DS} = 2.2 \Omega$ typ. ($V_{GS} = 2.5 \text{ V}$, $I_D = 50 \text{ mA}$)
- 2.5 V gate drive device.
- Small package (CMPAK)

Outline

CMPAK



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	100	mA
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	400	mA
Body-drain diode reverse drain current	I_{DR}	100	mA
Channel dissipation	Pch ^{Note 2}	300	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

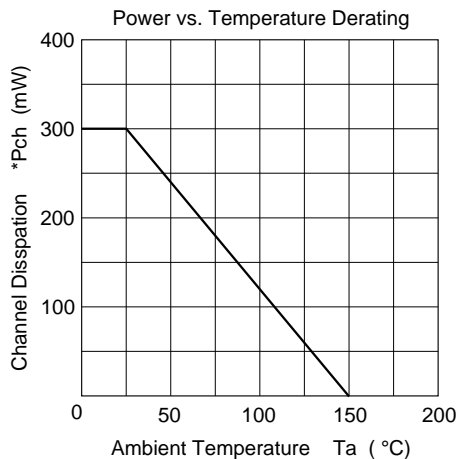
Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value on the alumina ceramic board (12.5x20x0.7mm)

Electrical Characteristics (Ta = 25°C)

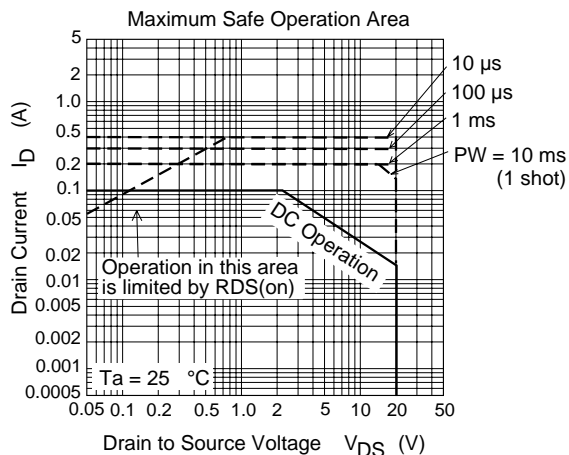
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D = 100 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±5	μA	$V_{GS} = \pm 8 V, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 20 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.8	—	1.8	V	$I_D = 10 \mu A, V_{DS} = 5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.6	1.9	Ω	$I_D = 50 mA, V_{GS} = 4 V$ ^{Note 3}
	$R_{DS(on)}$	—	2.2	3.2	Ω	$I_D = 50 mA, V_{GS} = 2.5 V$ ^{Note 3}
Forward transfer admittance	$ y_{fs} $	143	220	—	mS	$I_D = 50 mA, V_{DS} = 10 V$ ^{Note 3}
Input capacitance	Ciss	—	18	—	pF	$V_{DS} = 10 V$
Output capacitance	Coss	—	15	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	5	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	73	—	ns	$I_D = 50 mA, V_{GS} = 4 V$
Rise time	t_r	—	290	—	ns	$R_L = 200 \Omega$
Turn-off delay time	$t_{d(off)}$	—	360	—	ns	
Fall time	t_f	—	360	—	ns	

Note: 3. Pulse test
 4. Marking is CN

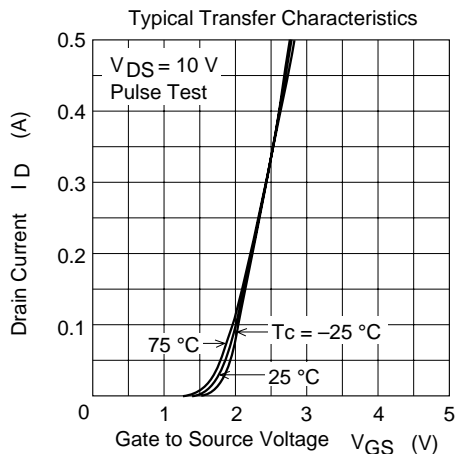
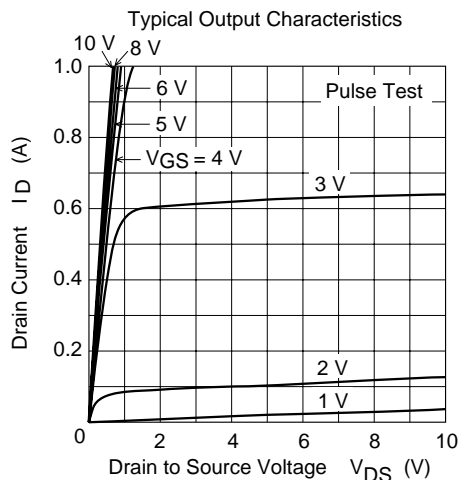
Main Characteristics



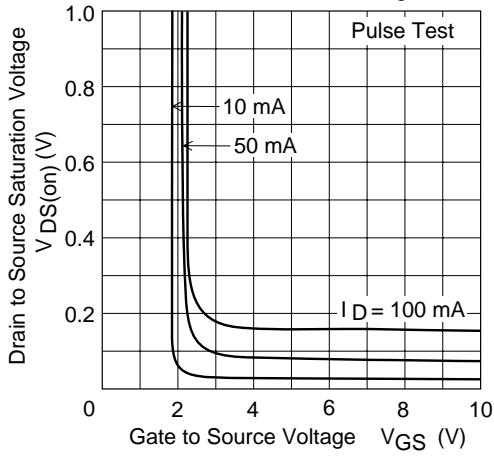
*Value on the alumina ceramic board.(12.5x20x0.7mm)



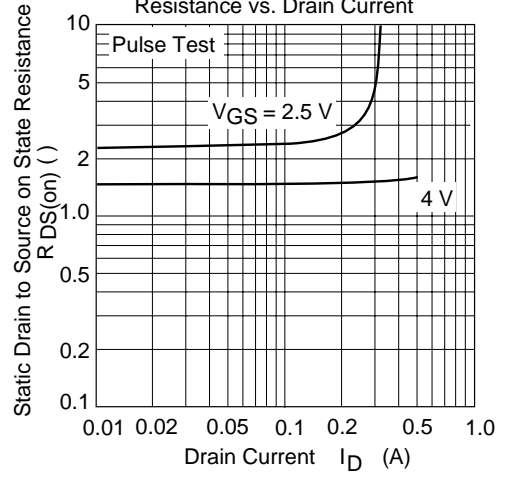
Value on the alumina ceramic board.(12.5x20x0.7mm)



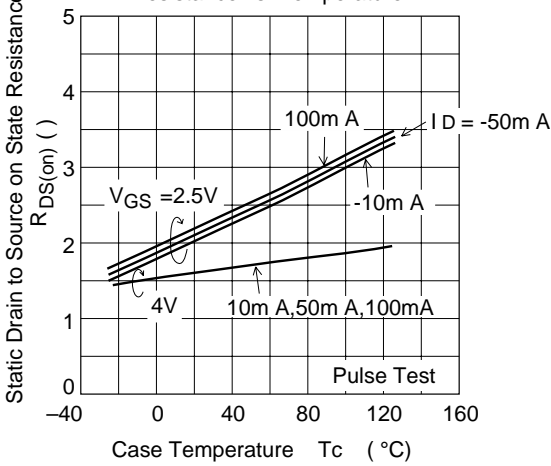
Drain to Source Saturation Voltage vs. Gate to Source Voltage



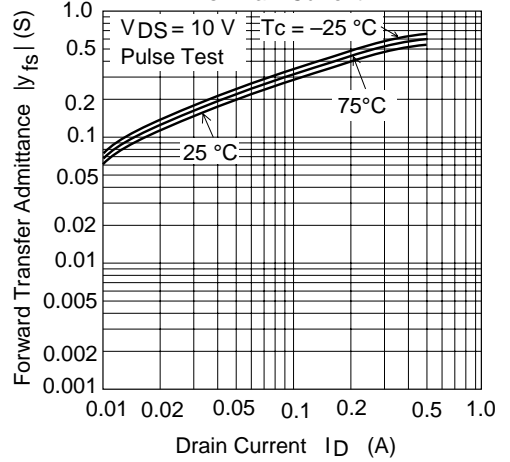
Static Drain to Source on State Resistance vs. Drain Current

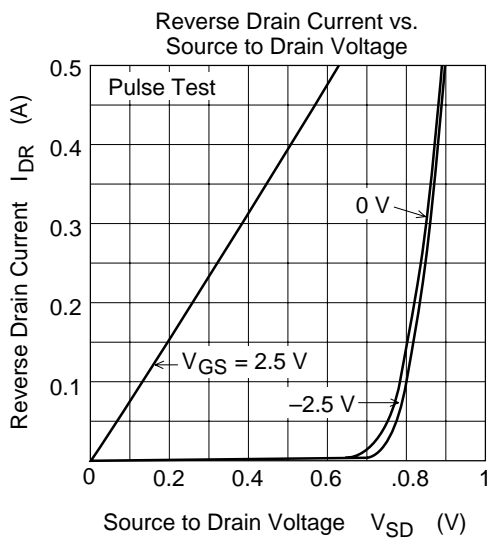
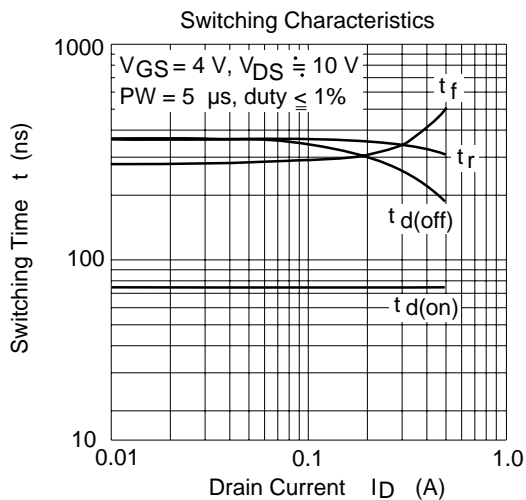
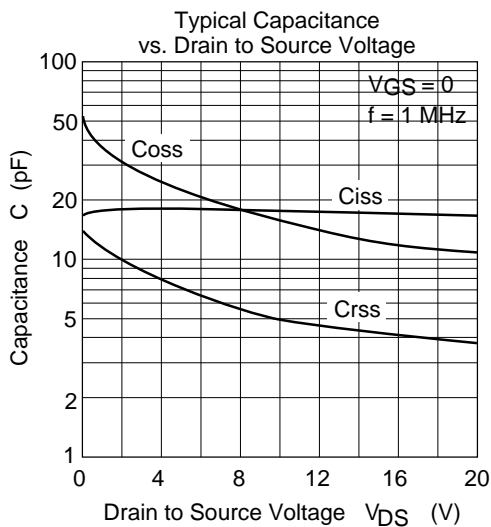


Static Drain to Source on State Resistance vs. Temperature

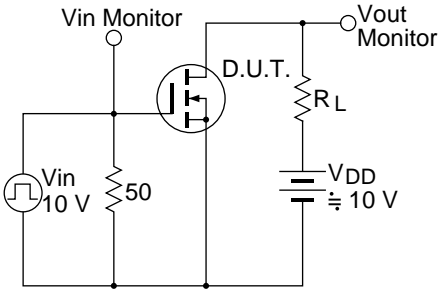


Forward Transfer Admittance vs. Drain Current

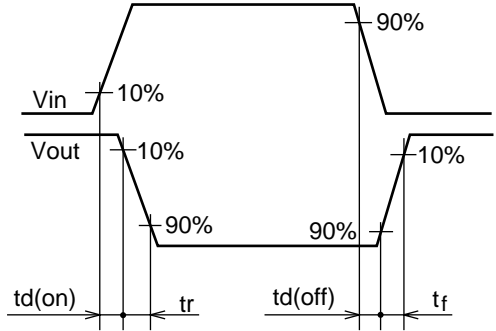




Switching Time Test Circuit



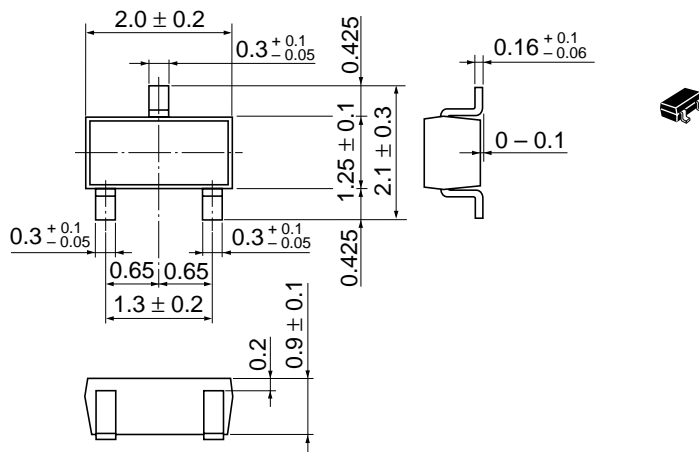
Waveforms



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	CMPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

Cautions

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : <http://semiconductor.hitachi.com/>
 Europe : <http://www.hitachi-eu.com/hel/ecg>
 Asia : <http://sicapac.hitachi-asia.com>
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
URL : <http://www.hitachi.com.hk>

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