

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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# 2SK3447

## Silicon N Channel Power MOS FET Power Switching

# RENESAS

ADE-208-1567E (Z)

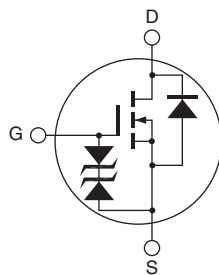
6th. Edition  
Dec. 2002

### Features

- Capable of 4 V gate drive
- Low drive current
- Low on-resistance
- $R_{DS(on)}=1.5 \Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )

### Outline

TO-92MOD.



1. Source
2. Drain
3. Gate

**Absolute Maximum Ratings**

(Ta = 25°C)

<b>Item</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>
Drain to source voltage	$V_{DSS}$	150	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	1	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	4	A
Body-drain diode reverse drain current	$I_{DR}$	1	A
Channel dissipation	$Pch$ <sup>Note2</sup>	0.9	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1 \%$ 

2. Value at Ta = 25°C

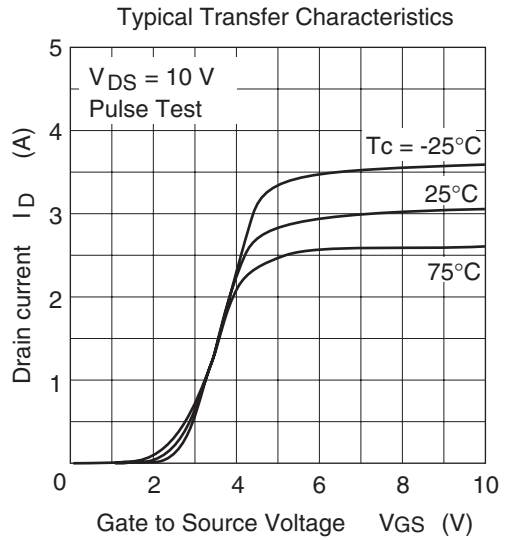
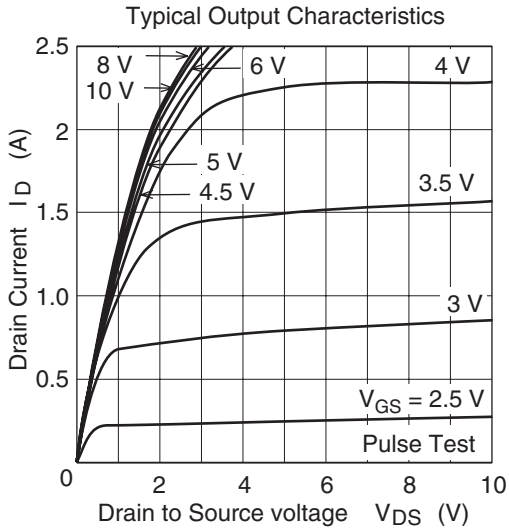
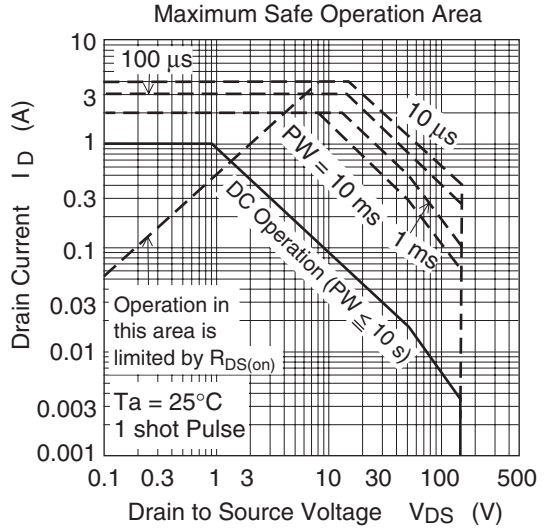
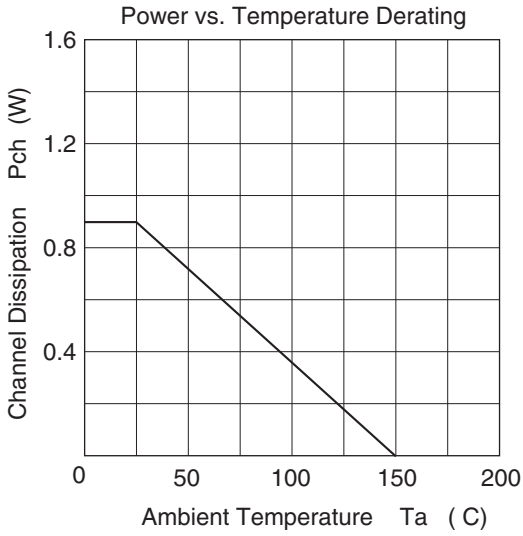
## Electrical Characteristics

(Ta = 25°C)

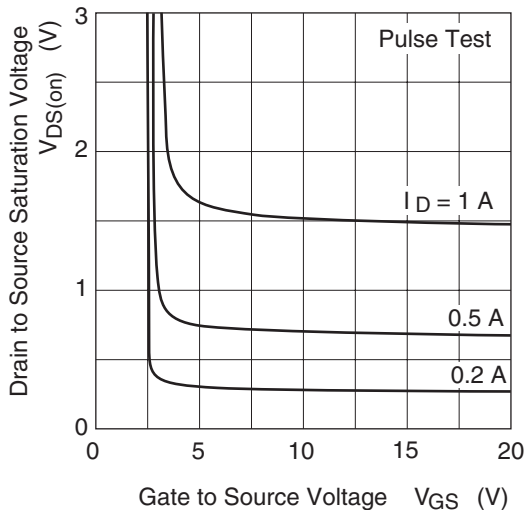
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	150	—	—	V	$I_D = 10\text{mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16\text{V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 150\text{V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10\text{V}$ , $I_D = 1\text{mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.5	1.95	$\Omega$	$I_D = 0.5\text{A}$ , $V_{GS} = 10\text{V}$ <sup>Note3</sup>
	$R_{DS(on)}$	—	1.9	2.5	$\Omega$	$I_D = 0.5\text{A}$ , $V_{GS} = 4\text{V}$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	0.5	0.9	—	S	$I_D = 0.5\text{A}$ , $V_{DS} = 10\text{V}$ <sup>Note3</sup>
Input capacitance	Ciss	—	85	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	Coss	—	36	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	18	—	pF	$f = 1\text{MHz}$
Total gate charge	Qg	—	4.5	—	nC	$V_{DD} = 100\text{V}$
Gate to source charge	Qgs	—	0.8	—	nC	$V_{GS} = 10\text{V}$
Gate to drain charge	Qgd	—	1.6	—	nC	$I_D = 1\text{A}$
Turn-on delay time	$t_{d(on)}$	—	7	—	ns	$V_{GS} = 10\text{V}$ , $I_D = 0.5\text{A}$
Rise time	$t_r$	—	6	—	ns	$R_L = 60\Omega$
Turn-off delay time	$t_{d(off)}$	—	21	—	ns	
Fall time	$t_f$	—	10	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	1.0	1.5	V	$I_F = 1\text{A}$ , $V_{GS} = 0$ <sup>Note3</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	60	—	ns	$I_F = 1\text{A}$ , $V_{GS} = 0$ $diF/dt = 100\text{A}/\mu\text{s}$

Notes: 3. Pulse test

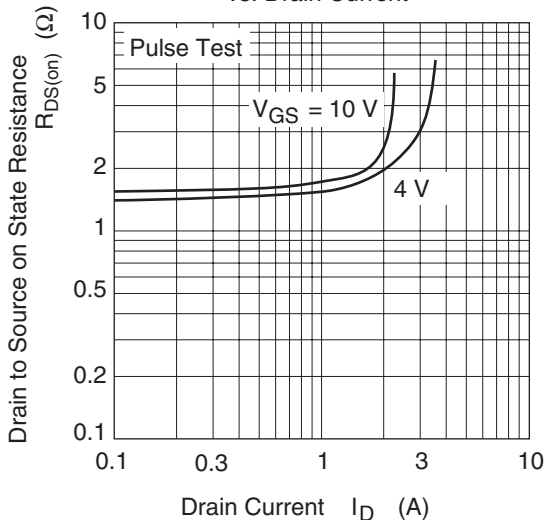
Main Characteristics



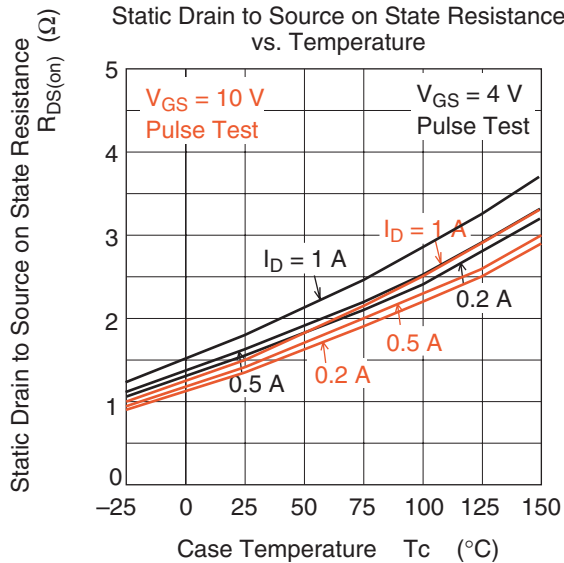
Drain to Source Saturation Voltage vs. Gate to Source Voltage



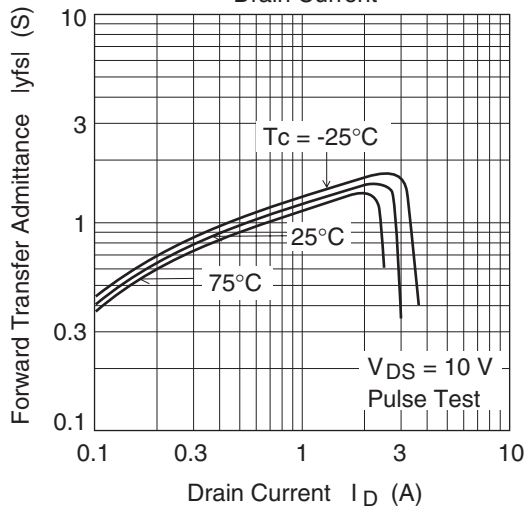
Static Drain to Source on State Resistance vs. Drain Current



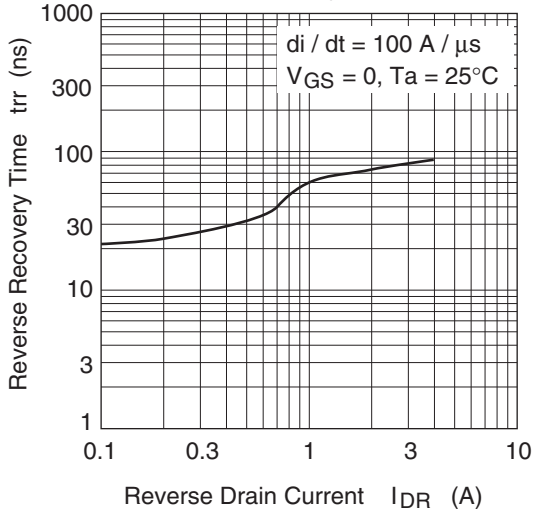
Static Drain to Source on State Resistance vs. Temperature



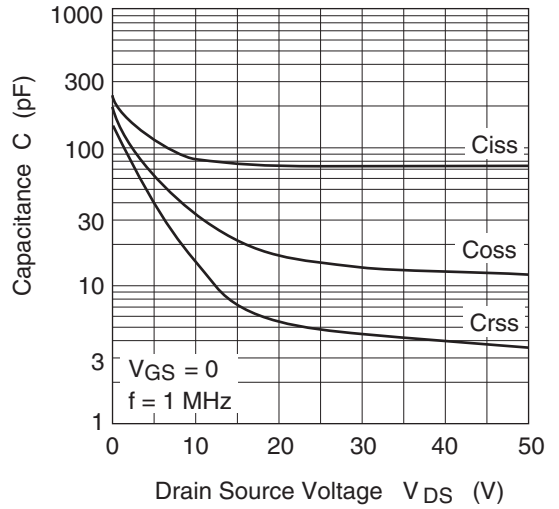
Forward Transfer Admittance vs. Drain Current



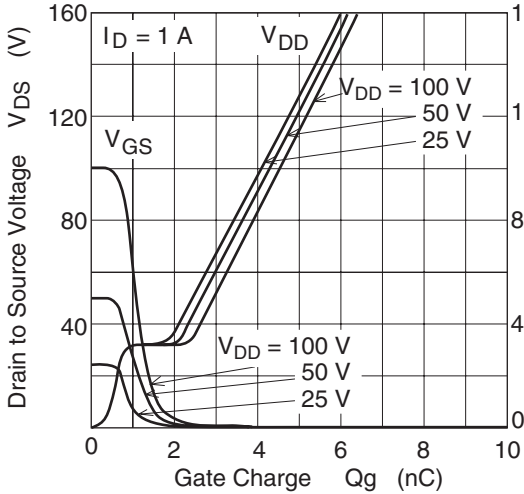
Body-Drain Diode Reverse Recovery Time



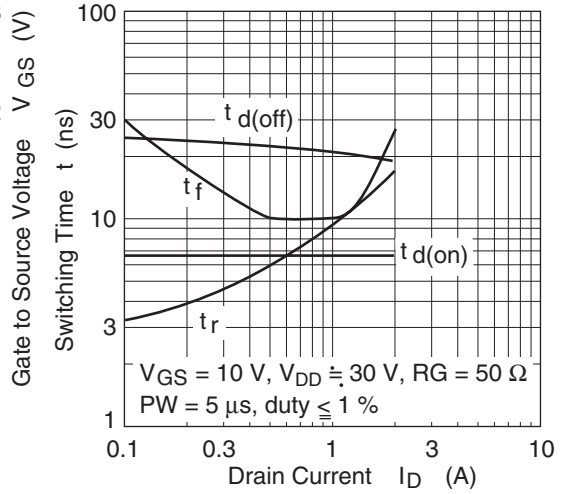
Typical Capacitance vs. Drain Source Voltage

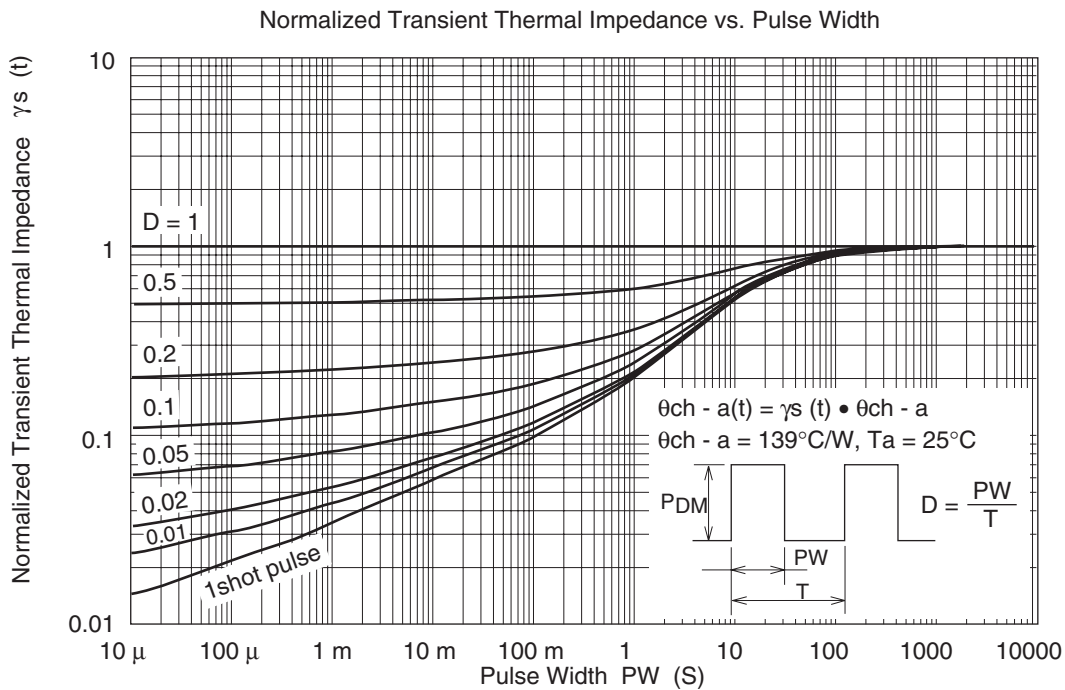
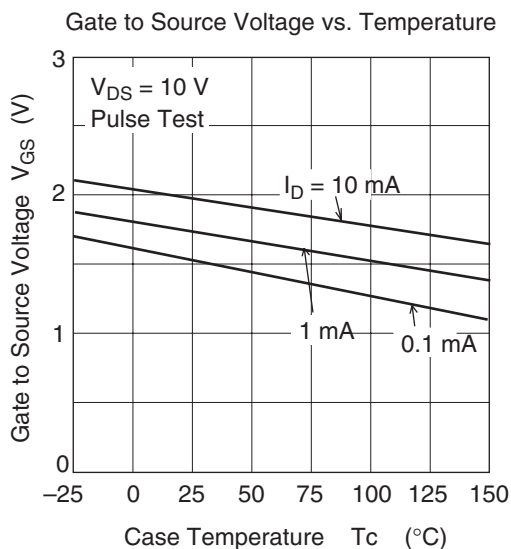
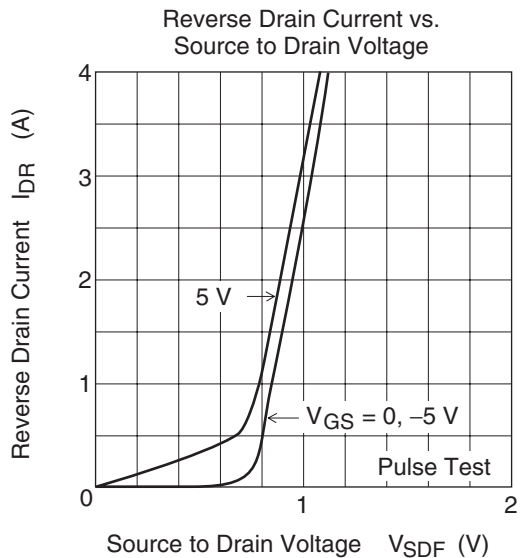


Dynamic Input Characteristics



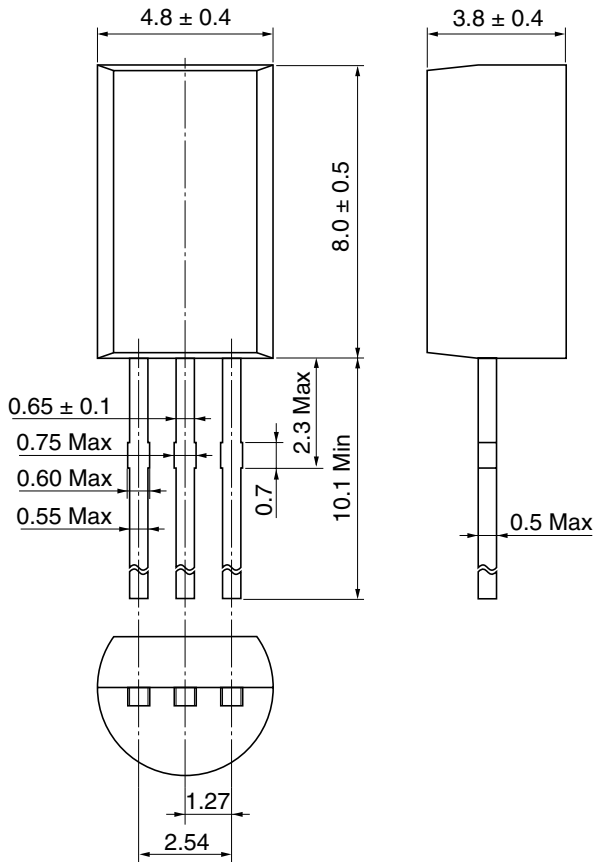
Switching Characteristics





Package Dimensions

As of July, 2002  
Unit: mm



Hitachi Code	TO-92 Mod
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.35 g

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# HITACHI

### Hitachi, Ltd.

Semiconductor & Integrated Circuits  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: <03> 3270-2111 Fax: <03> 3270-5109

URL <http://www.hitachisemiconductor.com/>

### For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
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Hitachi Europe Ltd.  
Electronic Components Group  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 778322

Hitachi Europe GmbH  
Electronic Components Group  
Dornacher Str 3  
D-85622 Feldkirchen  
Postfach 201, D-85619 Feldkirchen  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.  
Hitachi Tower  
16 Collyer Quay #20-00  
Singapore 049318  
Tel : <65>-6538-6533/6538-8577  
Fax : <65>-6538-6933/6538-3877  
URL : <http://semiconductor.hitachi.com.sg>

Hitachi Asia Ltd.  
(Taipei Branch Office)  
4/F, No. 167, Tun Hwa North Road  
Hung-Kuo Building  
Taipei (105), Taiwan  
Tel : <886>-(2)-2718-3666  
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Telex : 23222 HAS-TP  
URL : <http://semiconductor.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon Hong Kong  
Tel : <852>-2735-9218  
Fax : <852>-2730-0281  
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