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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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H7N0312LD, H7N0312LS, H7N0312LM

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

ADE-208-1572A(Z)

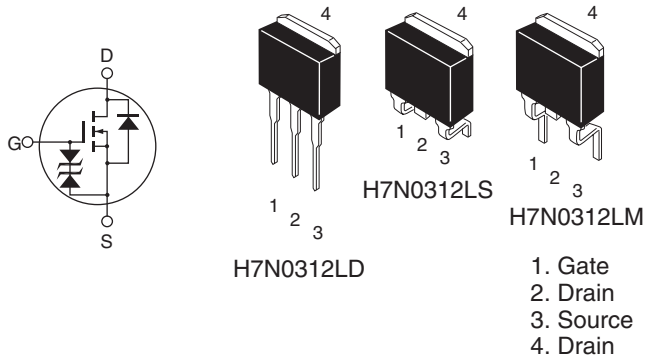
2nd. Edition
Aug. 2002

Features

- Low on-resistance
- $R_{DS(on)} = 2.6 \text{ m}\Omega$ typ.
- Low drive current
- 4.5 V gate drive device can be driven from 5 V source

Outline

LDPAK



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	85	A
Drain peak current	$I_{D(pulse)}$ Note 1	340	A
Body-drain diode reverse drain current	I_{DR}	85	A
Channel dissipation	P_{ch} Note 2	125	W
Channel to Case Thermal Impedance	θ_{ch-c}	1.0	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	−55 to +150	°C

Notes: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ C$

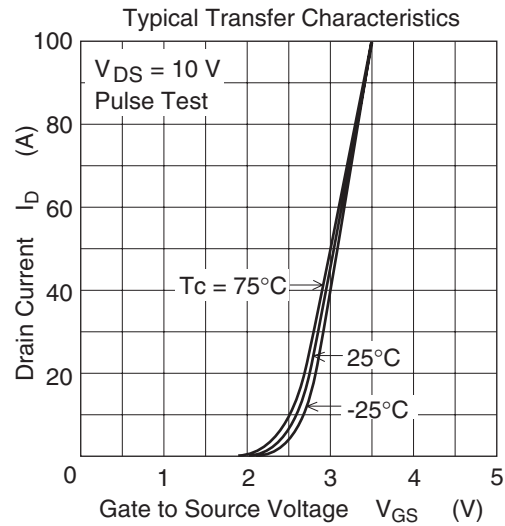
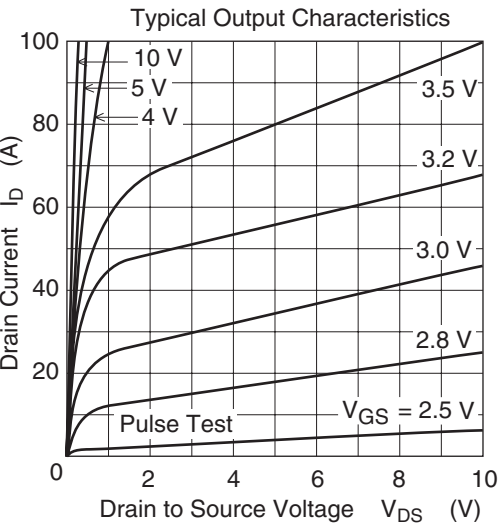
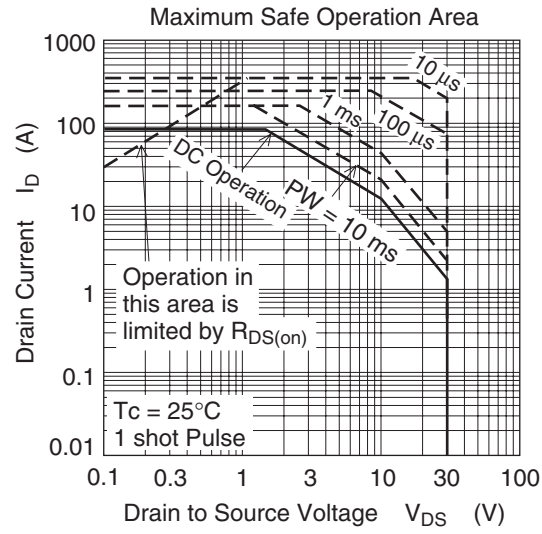
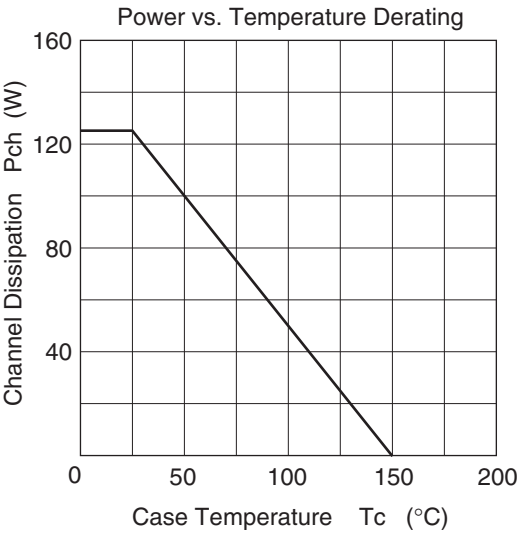
Electrical Characteristics

(Ta = 25°C)

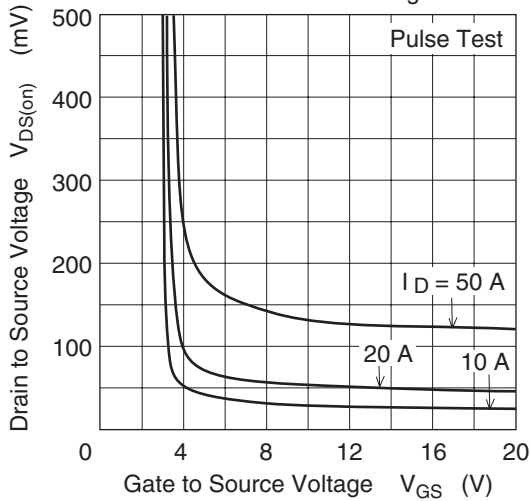
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$ ^{Note1}
Static drain to source on state resistance	$R_{DS(on)}$	—	2.6	3.3	$\text{m}\Omega$	$I_D = 42.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note1}
		—	4.0	5.8	$\text{m}\Omega$	$I_D = 42.5 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note1}
Forward transfer admittance	$ y_{fs} $	75	125	—	S	$I_D = 42.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note1}
Input capacitance	C_{iss}	—	6900	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	1750	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	820	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	115	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	24	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	24	—	nc	$I_D = 85 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	45	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 42.5 \text{ A}$
Rise time	t_r	—	380	—	ns	$R_L = 0.24 \text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	125	—	ns	$R_g = 4.7 \text{ }\Omega$
Fall time	t_f	—	50	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.92	—	V	$I_F = 85 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	75	—	ns	$I_F = 85 \text{ A}$, $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Notes: 1. Pulse test

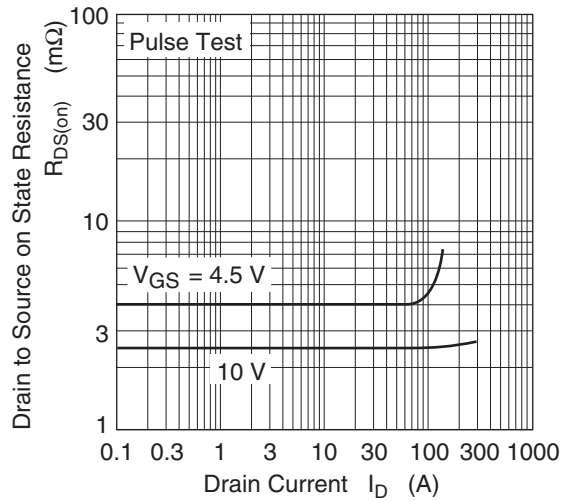
Main Characteristics



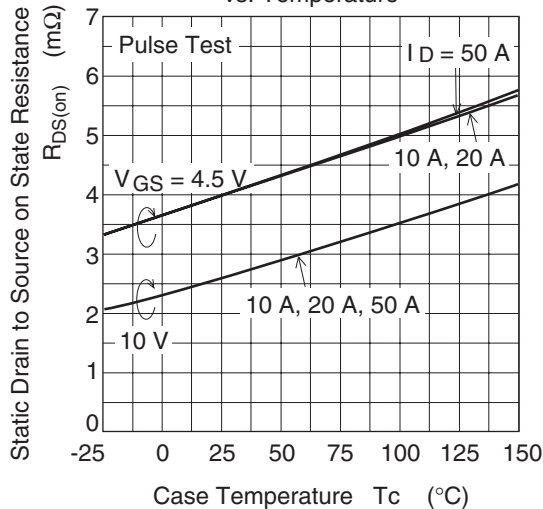
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



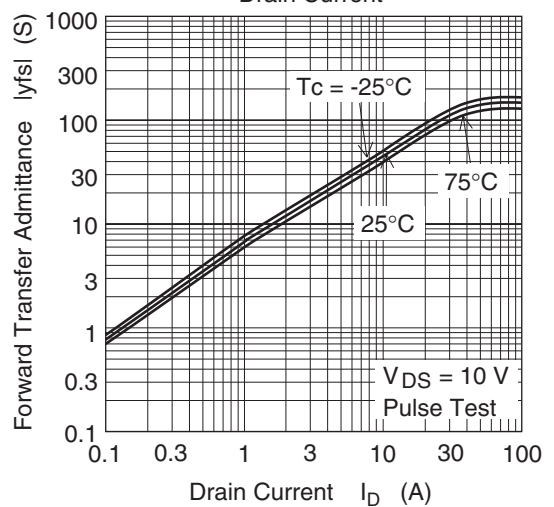
Static Drain to Source on State Resistance
vs. Drain Current



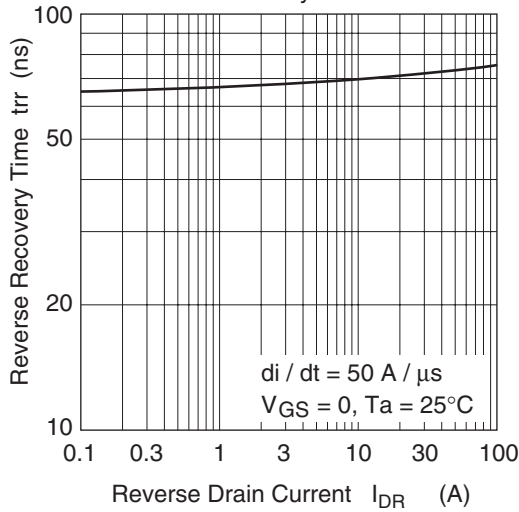
Static Drain to Source on State Resistance
vs. Temperature



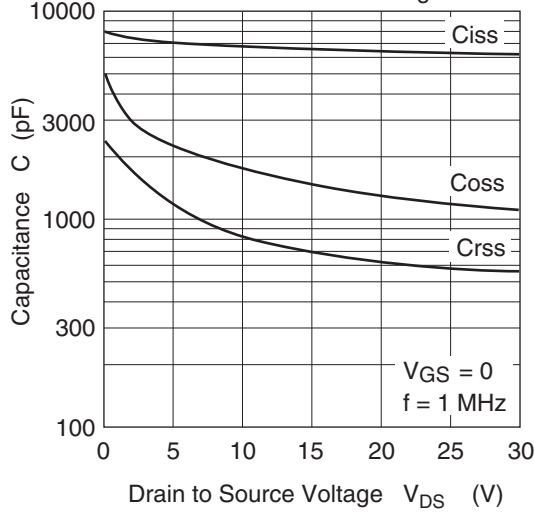
Forward Transfer Admittance vs.
Drain Current



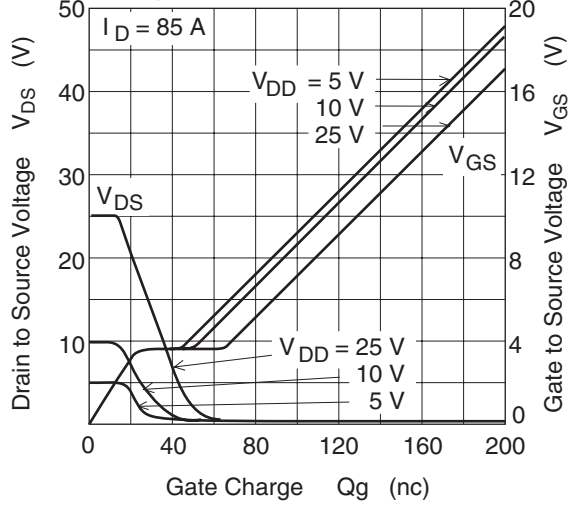
Body-Drain Diode Reverse Recovery Time



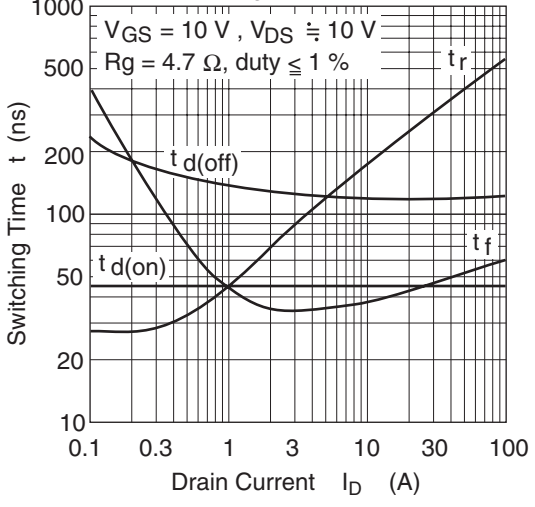
Typical Capacitance vs. Drain to Source Voltage

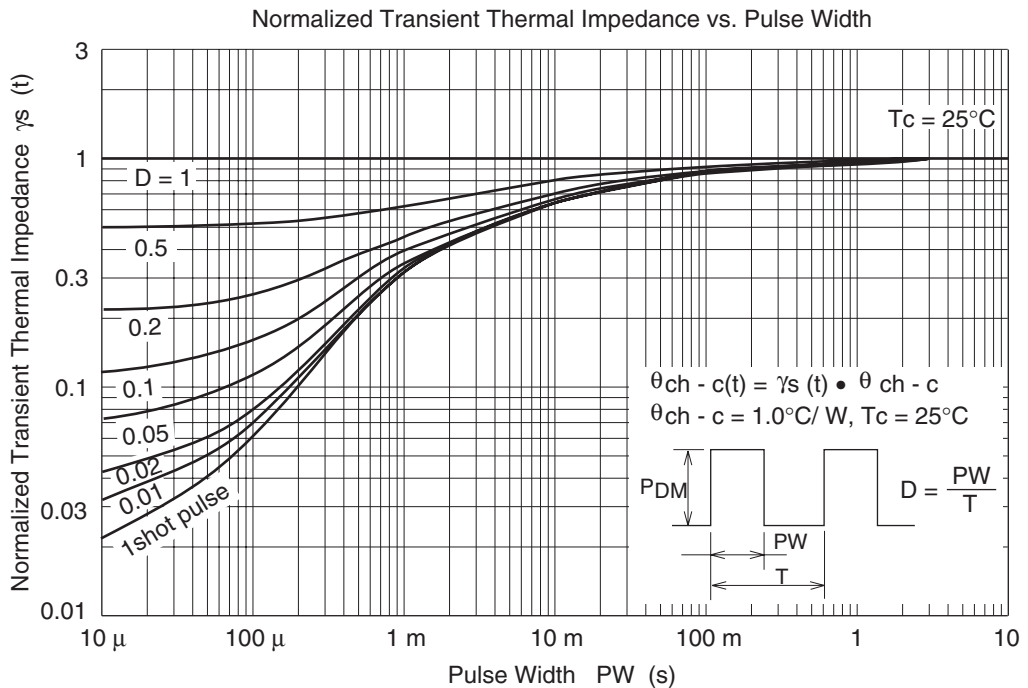
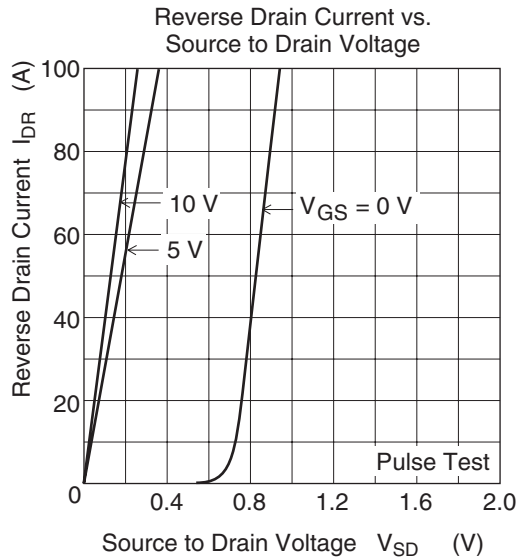


Dynamic Input Characteristics



Switching Characteristics

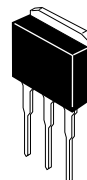
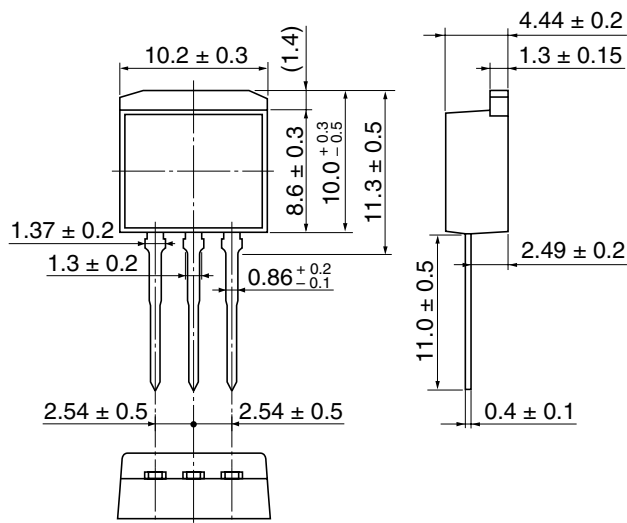




Package Dimensions

• H7N0312LD

Unit: mm

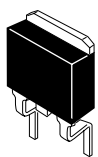
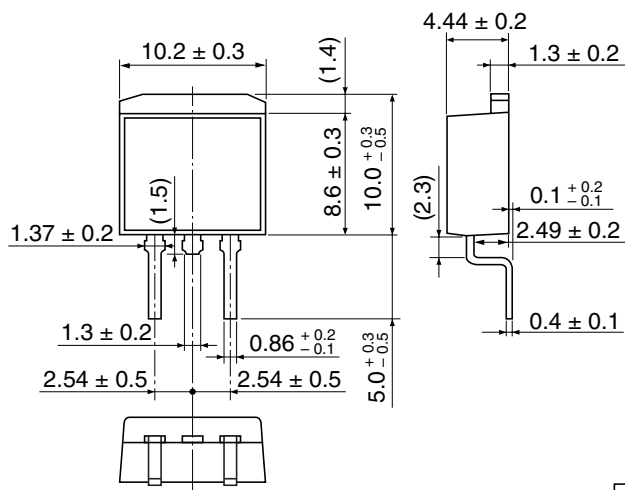


Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

H7N0312LD, H7N0312LS, H7N0312LM

• H7N0312LM

Unit: mm



Hitachi Code	LDBAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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