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Renesas Technology Corp. Customer Support Dept. April 1, 2003



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semiconductors may lead to personal injury, fire or property damage.
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measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or
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Dual Operational Amplifier



ADE-204-040 (Z) Rev. 0 Dec. 2000

Description

HA17458 is dual operational amplifiers which provides internal phase compensation and high performance. It can be applied widely to measuring control equipment and to general use.

Features

• High voltage gain: 100dB (Typ)

• Wide output amplitude: $\pm 13V$ (Typ) [at $R_L \ge 2k\Omega$]

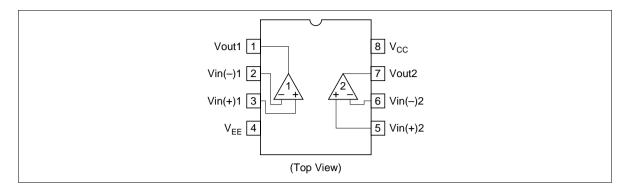
• Protected from output shortcircuit

· Internal phase compensation

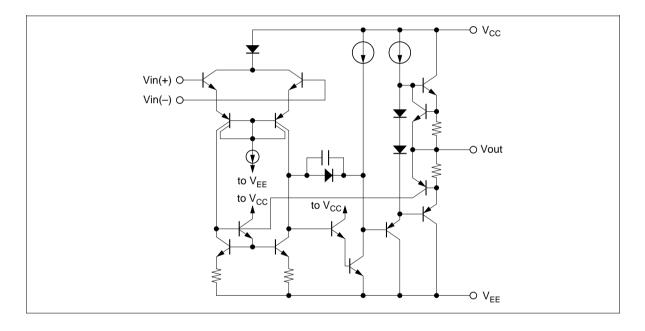
Ordering Information

Type No.	Application	Package		
HA17485FP	Industrial use	FP-8D		
HA17458F	Commercial use	FP-8D		
HA17458	Commercial use	DP-8		
HA17458PS	Industrial use	DP-8		

Pin Arrangement



Circuit Schematic (1/2)



Absolute Maximum Ratings $(Ta = 25^{\circ}C)$

R	ati	in	a	s

Item	Symbol	HA17458	HA17458PS	HA17458F	HA17458FP	Unit
Supply voltage	V_{cc}	+18	+18	+18	+18	V
	V _{EE}	-18	-18	-18	-18	V
Intput voltage	V _{IN} *3	±15	±15	±15	±15	V
Differential input voltage	$V_{IN(diff)}$	±30	±30	±30	±30	V
Power dissipation	P _T	670*1	670*1	385*2	385*2	mW
Operating temperature	Topr	-20 to +75	-20 to +75	-20 to +75	-20 to +75	°C
Storage temperature	Tstg	-55 to +125	-55 to +125	-55 to +125	-55 to +125	°C

Notes: 1. These are the allowable values up to Ta = 45 °C. Derate by 8.3mW/°C above that temperature.

- 2. These are the allowable values up to Ta = 31 $^{\circ}$ C mounting on 30% wiring density glass epoxy board. Derate by 7.14mW/ $^{\circ}$ C above that temperature.
- 3. If the supply voltage is less than $\pm 15V$, input voltage should be less than supply voltage.

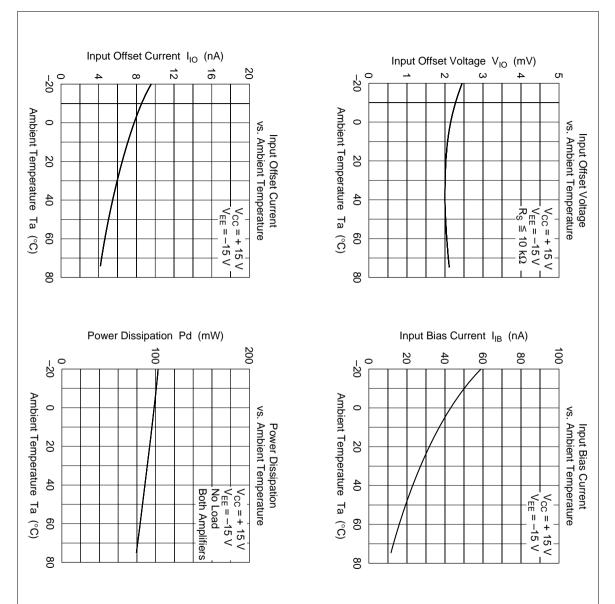
Electrical Characteristics 1 ($V_{CC} = -V_{EE} = 15V$, $Ta = 25^{\circ}C$)

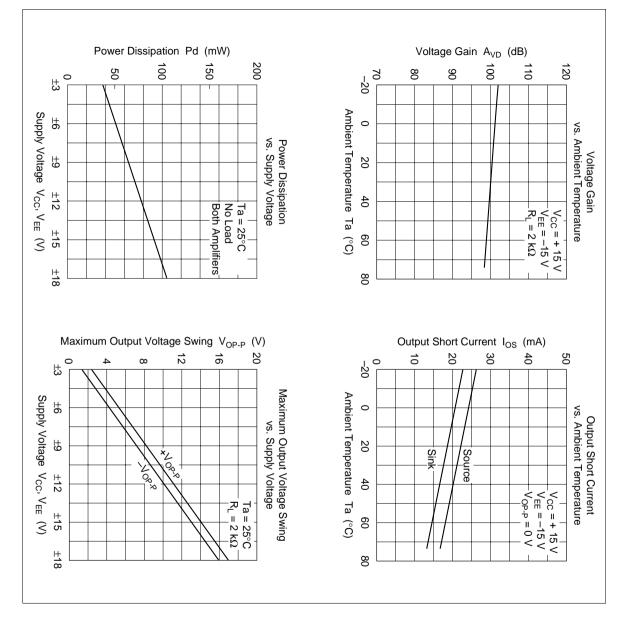
Item	Symbol	Min	Тур	Max	Unit	Test conditions
Input offset voltage	V _{IO}	_	2.0	6.0	mV	$R_S \le 10k\Omega$
Input offset current	I _{IO}	_	6	200	nA	
Input bias current	I _{IB}	_	30	500	nA	
Line regulation	$\Delta V_{IO}/\Delta V_{CC}$	_	30	150	μV/V	$R_s \le 10k\Omega$
	$\Delta V_{IO}/\Delta V_{EE}$	_	30	150	μV/V	$R_{s} \le 10k\Omega$
Voltage gain	A _{VD}	86	100	_	dB	$R_L \ge 2k\Omega$, Vout = $\pm 10V$
Common mode rejection ratio	CMR	70	90	_	dB	$R_s \le 10k\Omega$
Common mode input voltage range	V _{CM}	±12	±13	_	V	
Peak-to-peak output voltage	Vop-p	±12	±14	_	V	$R_L = 10k\Omega$
Power dissipation	P _d	_	90	200	mW	No load, 2 channel
Slew rate	SR	_	0.6	_	V/µs	A _{VD} = 1
Input resistance	Rin	0.3	1.0	_	$M\Omega$	
Input capacitance	Cin	_	6.0	_	pF	
Output resistance	Rout		75		Ω	

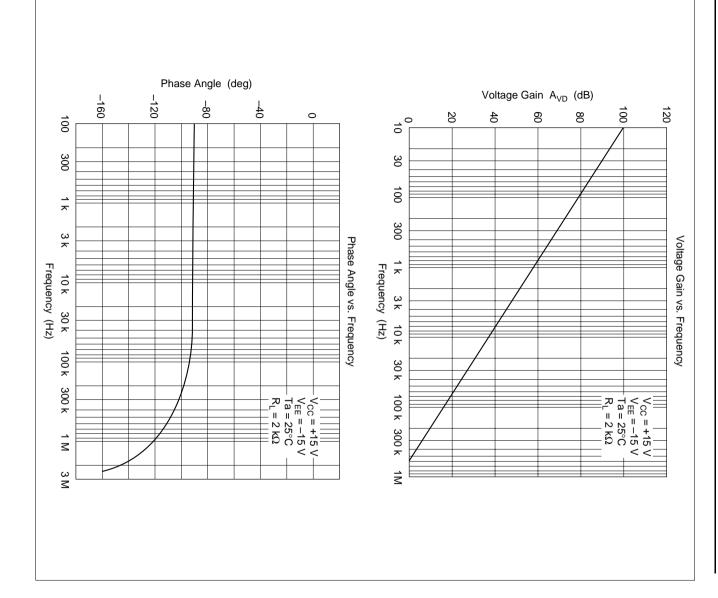
Electrical Characteristics 2 ($V_{CC} = -V_{EE} = 15V$, Ta = -20 to $+75^{\circ}C$)

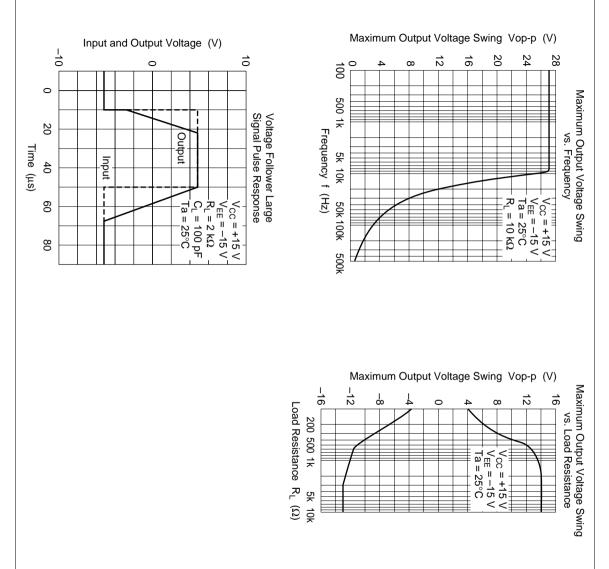
Item	Symbol	Min	Тур	Max	Unit	Test conditions
Input offset voltage	V _{IO}	_	_	9.0	mV	$R_s \le 10k\Omega$
Input offset current	I _{IO}	_	_	400	nΑ	
Input bias current	I _{IB}	_	_	1100	nA	
Voltage gain	A_{VD}	80	_	_	dB	$R_L \ge 2k\Omega$, Vout = $\pm 10V$
Peak-to-peak output voltage	Vop-p	±10	±13	_	V	$R_L = 2k\Omega$

Characteristic Curves



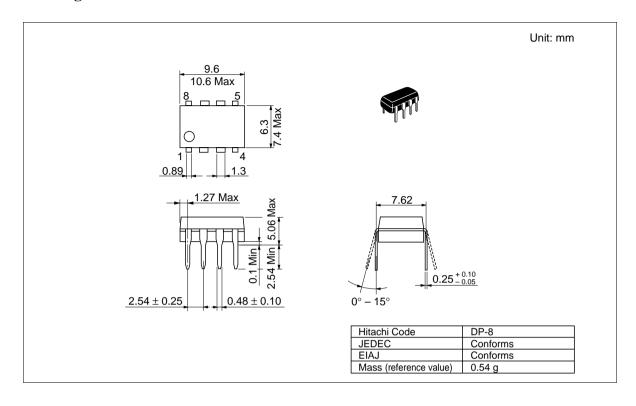


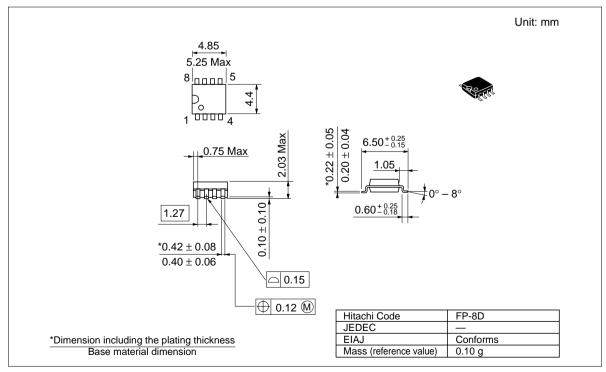




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Package Dimensions





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