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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HAT1016R

Silicon P Channel Power MOS FET High Speed Power Switching

RENESAS

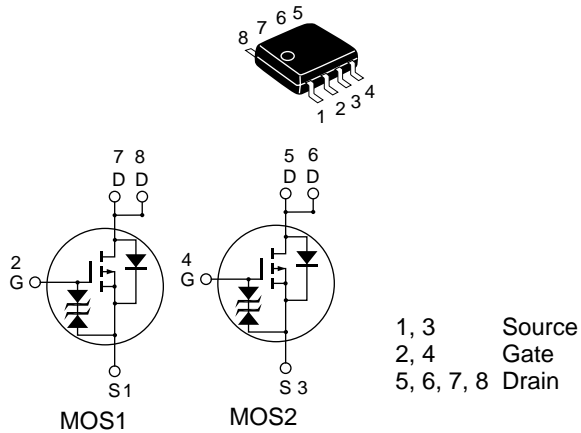
ADE-208-471E (Z)
6th. Edition
Feb. 1999

Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

Outline

SOP-8



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	- 30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	- 4.5	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	- 36	A
Body-drain diode reverse drain current	I_{DR}	- 4.5	A
Channel dissipation	Pch ^{Note2}	2	W
Channel dissipation	Pch ^{Note3}	3	W
Channel temperature	Tch	150	°C
Storage temperature	$Tstg$	- 55 to + 150	°C

Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$

2. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

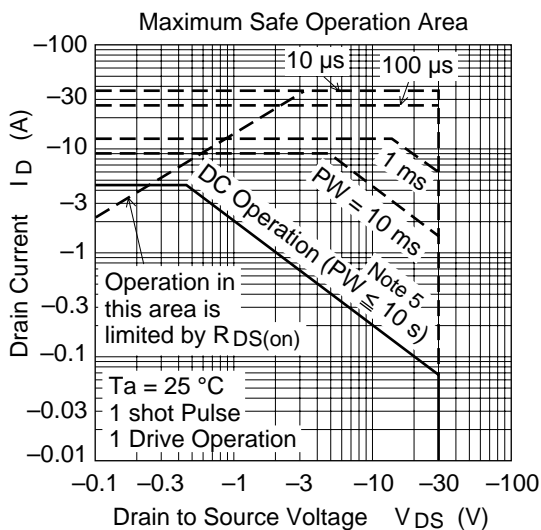
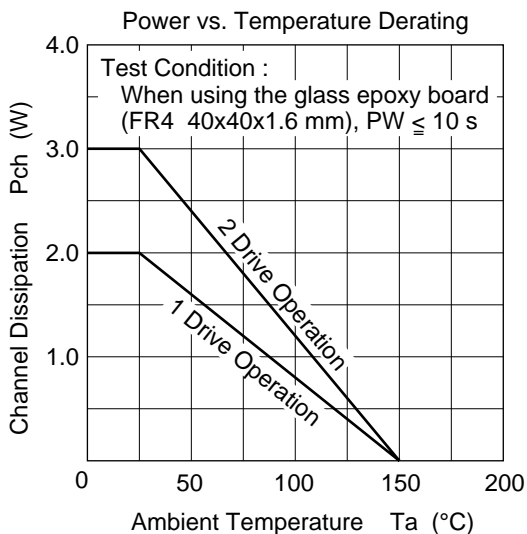
3. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

Electrical Characteristics (Ta = 25°C)

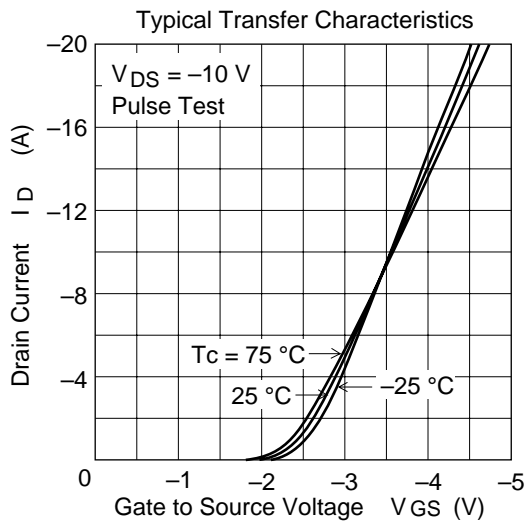
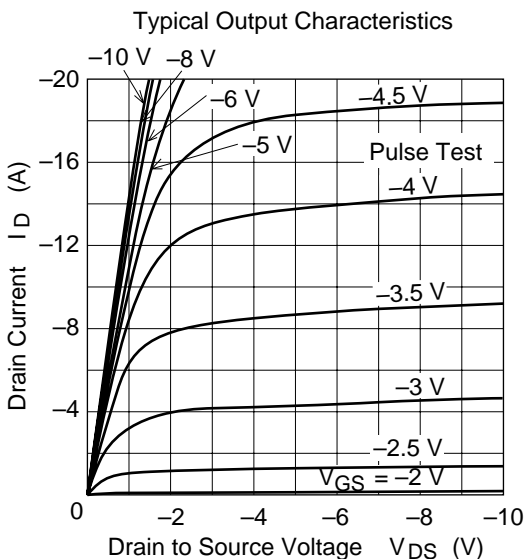
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10\text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100\ \mu A$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16\text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -30\text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10\text{ V}$, $I_D = -1\text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.07	0.09	Ω	$I_D = -3\text{ A}$, $V_{GS} = -10\text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	4	6	—	S	$I_D = -3\text{ A}$, $V_{DS} = -10\text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	660	—	pF	$V_{DS} = -10\text{ V}$
Output capacitance	C_{oss}	—	440	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	140	—	pF	$f = 1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	24	—	ns	$V_{GS} = -4\text{ V}$, $I_D = -3\text{ A}$
Rise time	t_r	—	165	—	ns	$V_{DD} \cong -10\text{ V}$
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	70	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-0.9	-1.4	V	$I_F = -4.5\text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	60	—	ns	$I_F = -4.5\text{ A}$, $V_{GS} = 0$ $diF/dt = 20\text{ A}/\mu s$

Note: 4. Pulse test

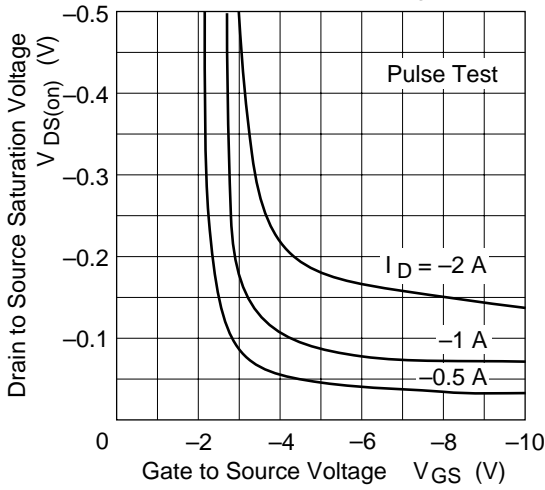
Main Characteristics



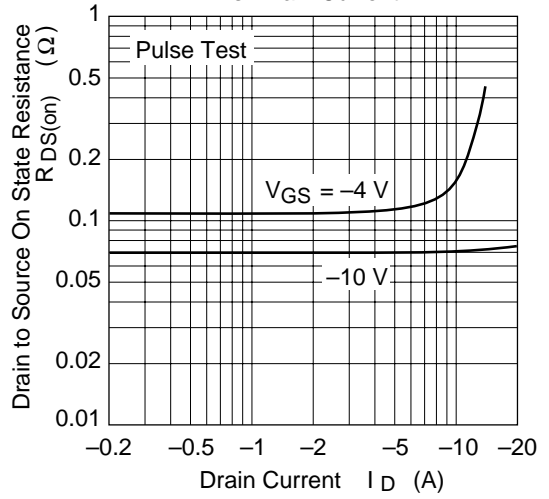
Note 5 :
When using the glass epoxy board (FR4 40 x 40 x 1.6 mm)



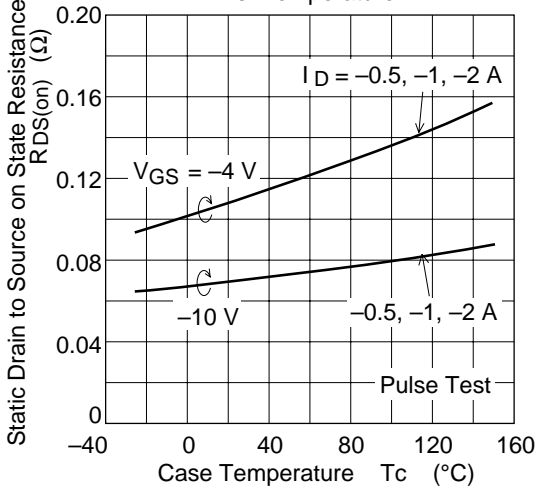
Drain to Source Saturation Voltage vs. Gate to Source Voltage



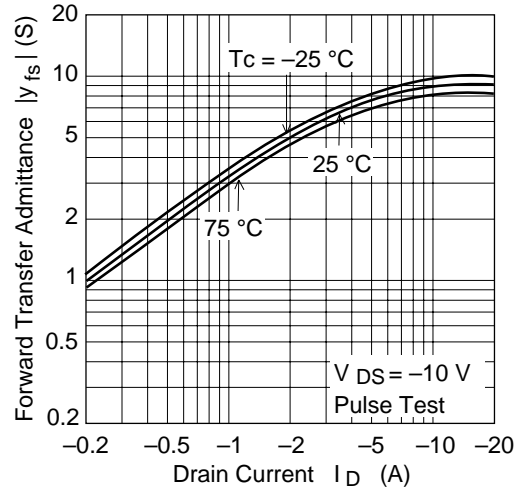
Static Drain to Source on State Resistance vs. Drain Current



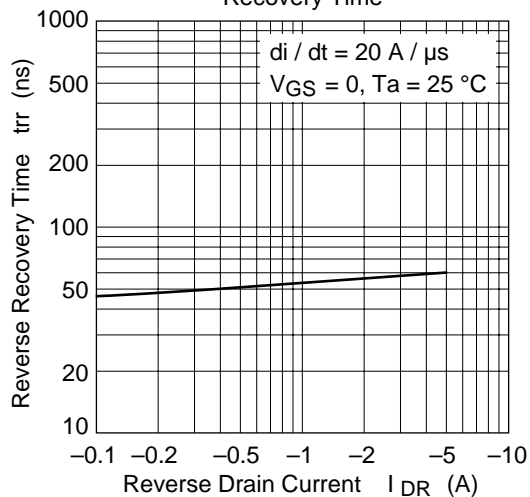
Static Drain to Source on State Resistance vs. Temperature



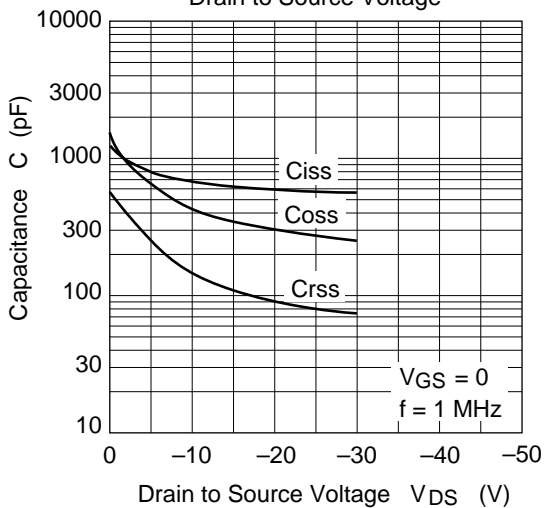
Forward Transfer Admittance vs. Drain Current



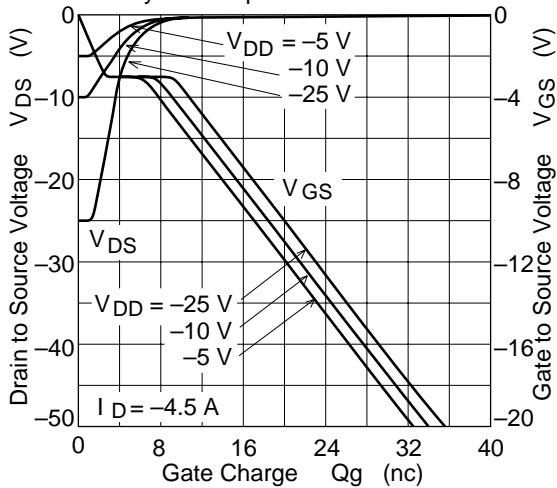
Body-Drain Diode Reverse Recovery Time



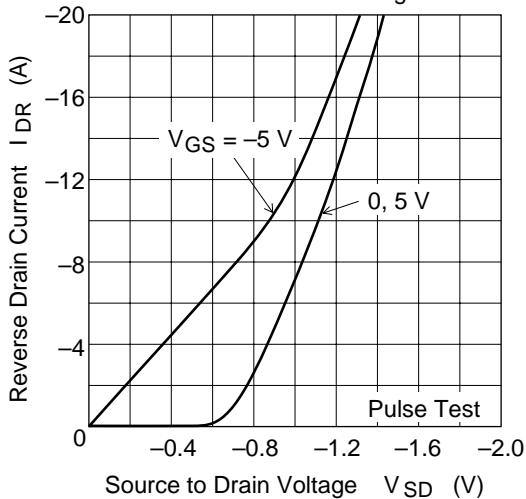
Typical Capacitance vs. Drain to Source Voltage

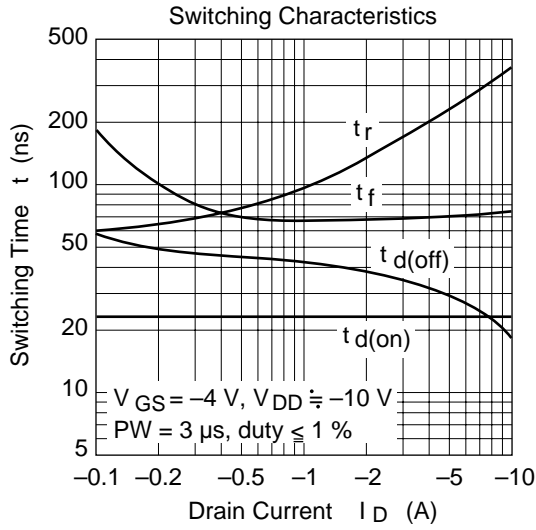


Dynamic Input Characteristics

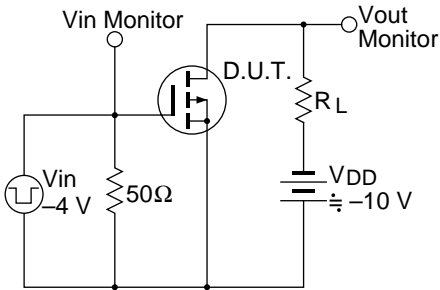


Reverse Drain Current vs. Source to Drain Voltage

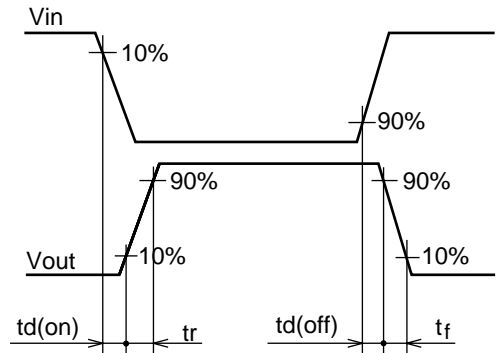


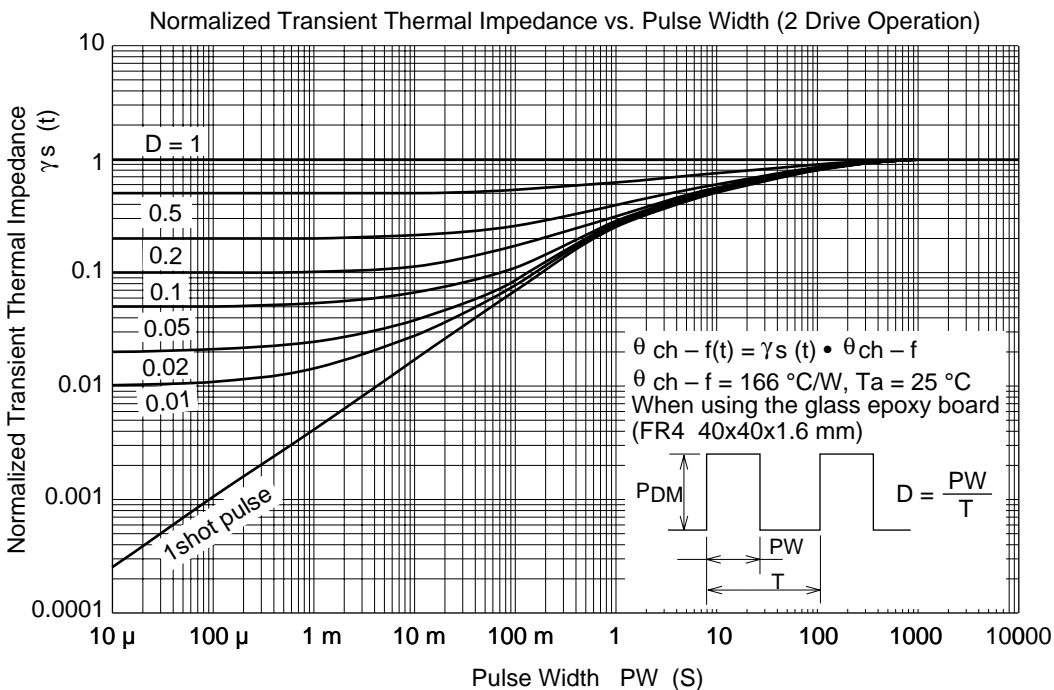
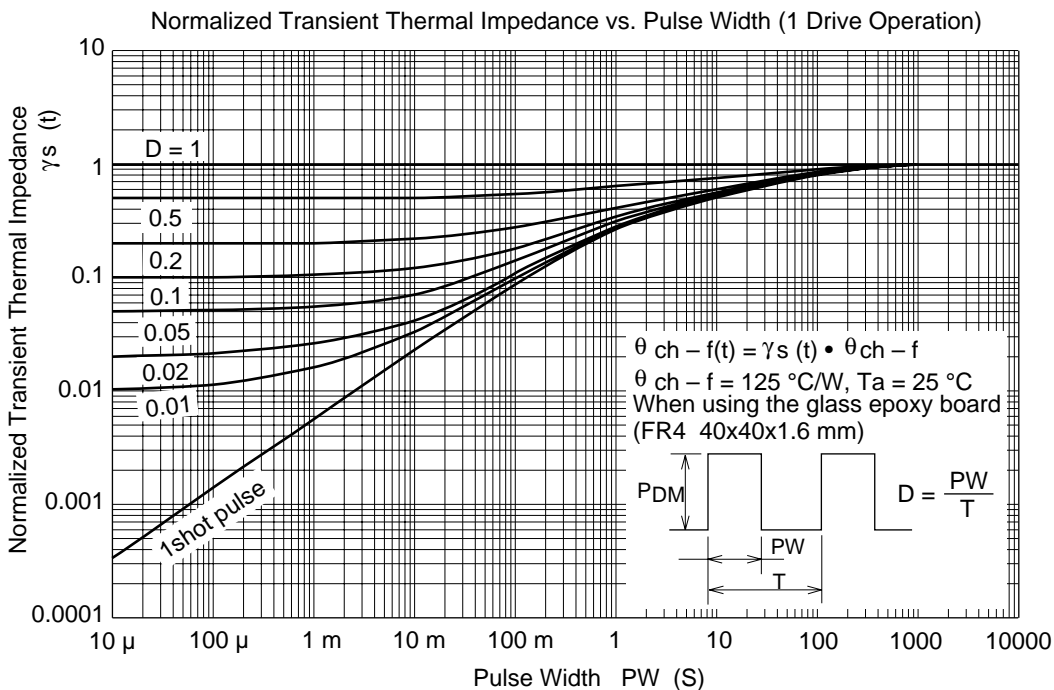


Switching Time Test Circuit



Switching Time Waveform

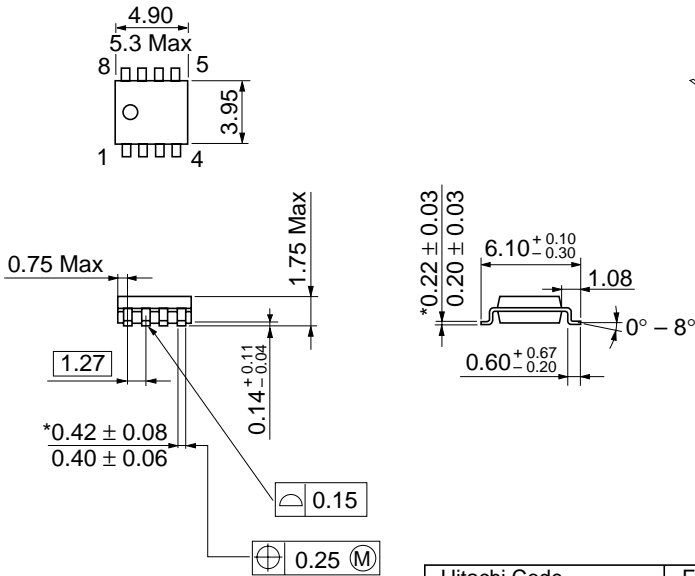




Package Dimensions

As of January, 2001

Unit: mm



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : <http://semiconductor.hitachi.com/>
 Europe : <http://www.hitachi-eu.com/hel/ecg>
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
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