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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HAT1043M

Silicon P Channel Power MOS FET
Power Switching

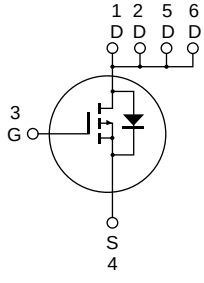
ADE-208-754D (Z)
5th Edition
Feb. 1999

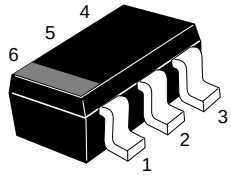
Features

- Low on-resistance
- Low drive current
- High density mounting
- 2.5 V gate drive device can be driven from 3 V source

Outline

TSOP–6





4	Source
3	Gate
1, 2, 5, 6	Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±12	V
Drain current	I_D	–4.4	A
Drain peak current	$I_{D(pulse)}$ Note 1	–17.6	A
Body-drain diode reverse drain current	I_{DR} Note 2	–4.4	A
Channel dissipation	$Pch_{(pulse)}$ Note 2	2.0	W
	$Pch_{(continuous)}$ Note 3	1.05	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. When using the alumina ceramic board (50 x 50 x 0.7 mm), PW ≤ 5 s, Ta = 25°C
3. When using the alumina ceramic board (50 x 50 x 0.7 mm), Ta = 25°C

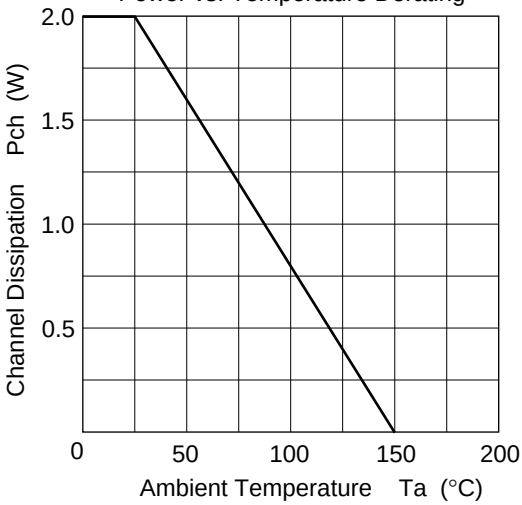
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	µA	V_{GS} = ±12 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	–1	µA	V_{DS} = –20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.4	—	–1.4	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	55	65	mΩ	I_D = –3 A, V_{GS} = –4.5 V Note 1
		—	85	110	mΩ	I_D = –3 A, V_{GS} = –2.5 V Note 1
Forward transfer admittance	$\|y_{fs}\|$	4	7	—	S	I_D = –3 A, V_{DS} = –10 V Note 1
Input capacitance	Ciss	—	750	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	310	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	220	—	pF	f = 1 MHz
Total Gate charge	Qg	—	11	—	nc	V_{DD} = –10 V
Gate to Source charge	Qgs	—	2	—	nc	V_{GS} = –4.5 V
Gate to Drain charge	Qgd	—	3.5	—	nc	I_D= –4.4 A
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	V_{GS} = –4.5 V, I_D = –3 A
Rise time	t_r	—	100	—	ns	R_L = 3.3 Ω
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	t_f	—	100	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.95	–1.23	V	I_F = –4.4 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	50	—	ns	I_F = –4.4 A, V_{GS} = 0 diF/ dt = –20 A/ µs

Note: 1. Pulse test

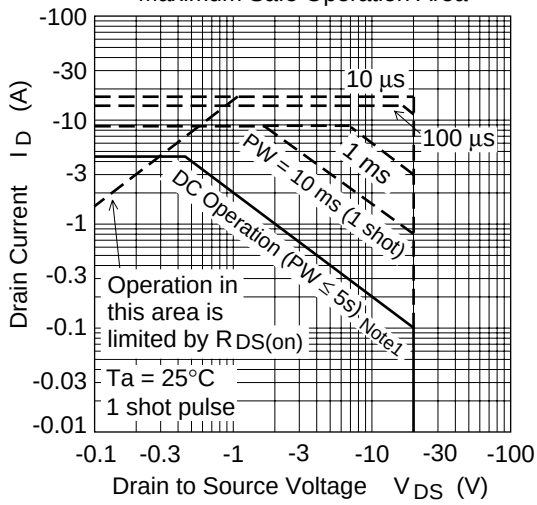
Main Characteristics

Power vs. Temperature Derating



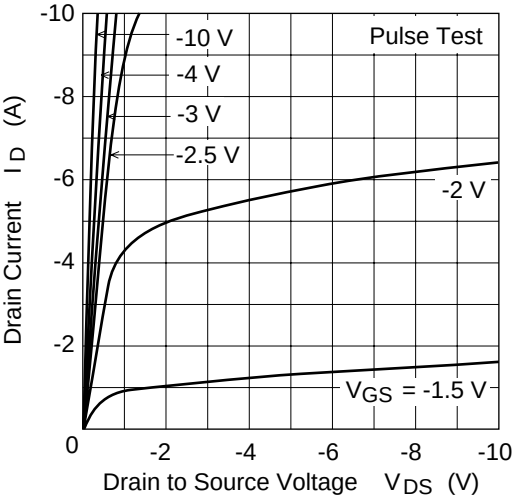
Test Condition
When using the alumina ceramic board (50x50x0.7mm),(PW ≤ 5s)

Maximum Safe Operation Area

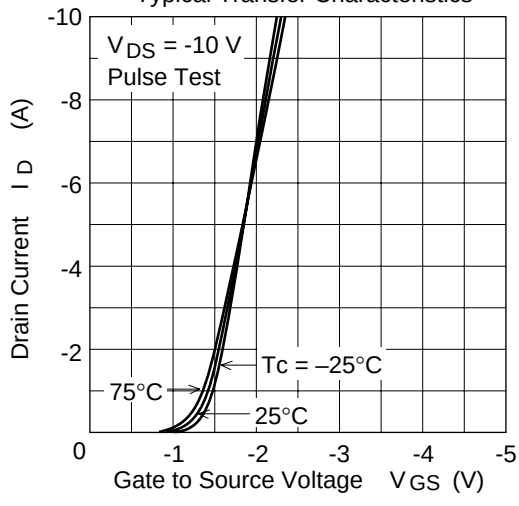


Note 1 When using the alumina ceramic board (50x50x0.7mm)

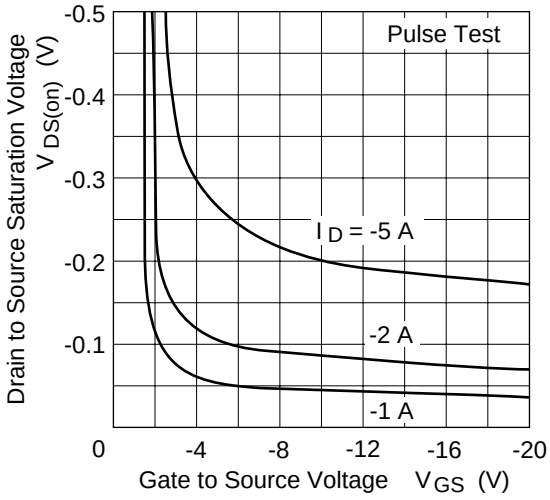
Typical Output Characteristics



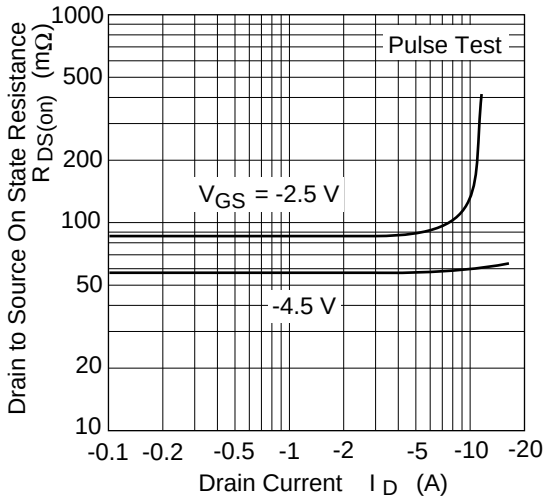
Typical Transfer Characteristics



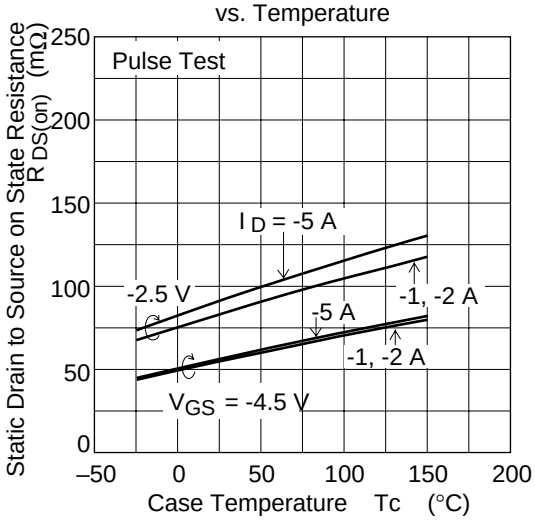
Drain to Source Saturation Voltage vs. Gate to Source Voltage



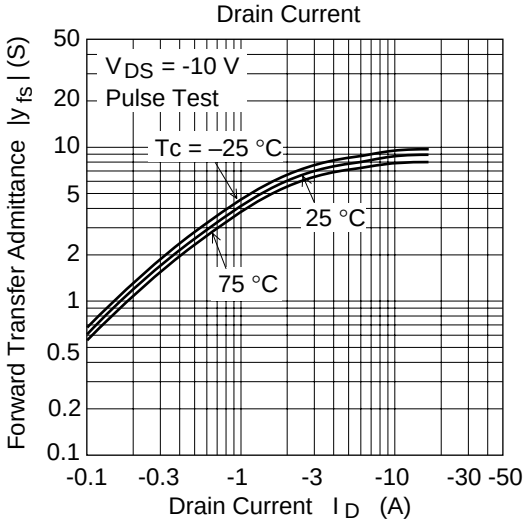
Static Drain to Source on State Resistance vs. Drain Current



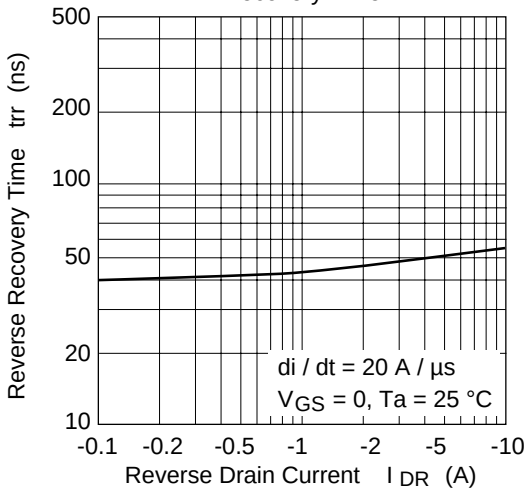
Static Drain to Source on State Resistance vs. Temperature



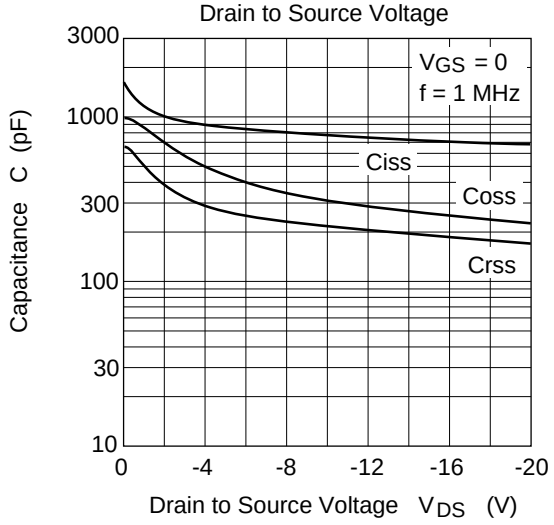
Forward Transfer Admittance vs. Drain Current



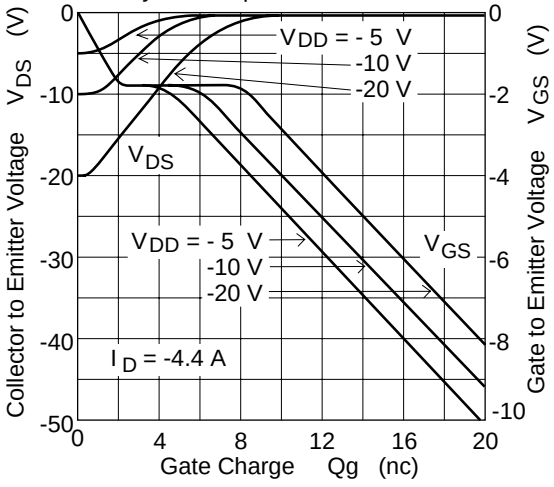
Body–Drain Diode Reverse Recovery Time



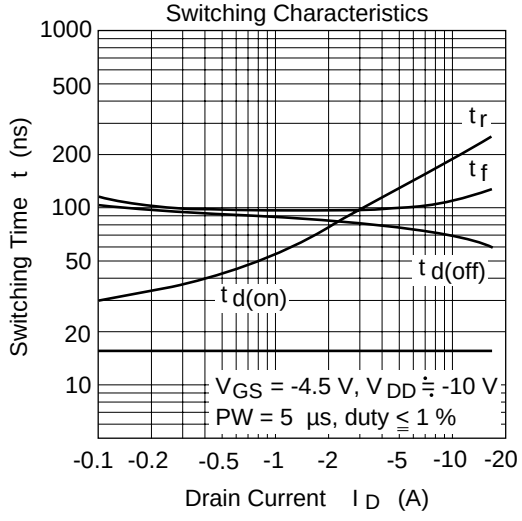
Typical Capacitance vs. Drain to Source Voltage



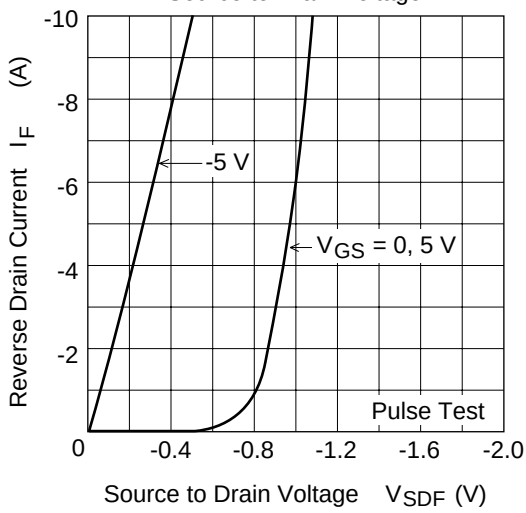
Dynamic Input Characteristics



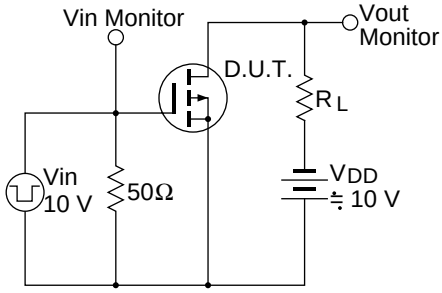
Switching Characteristics



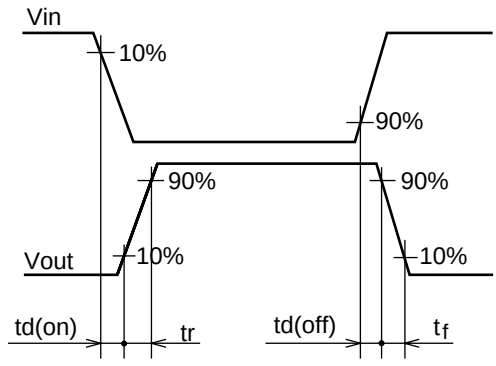
Reverse Drain Current vs.
Source to Drain Voltage

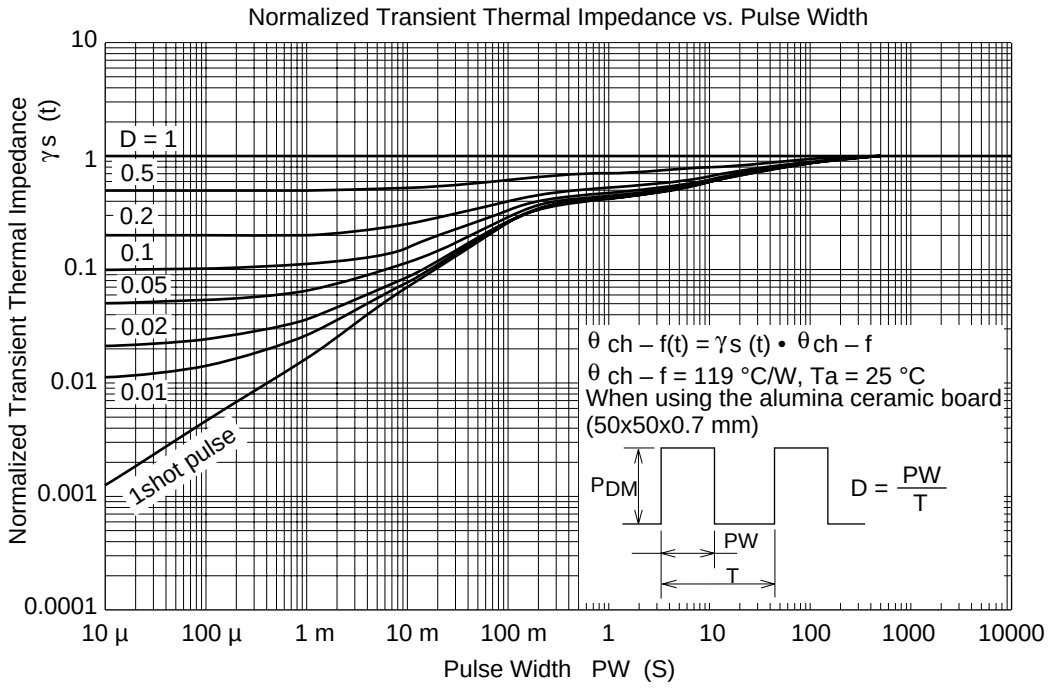


Switching Time Test Circuit



Switching Time Waveform

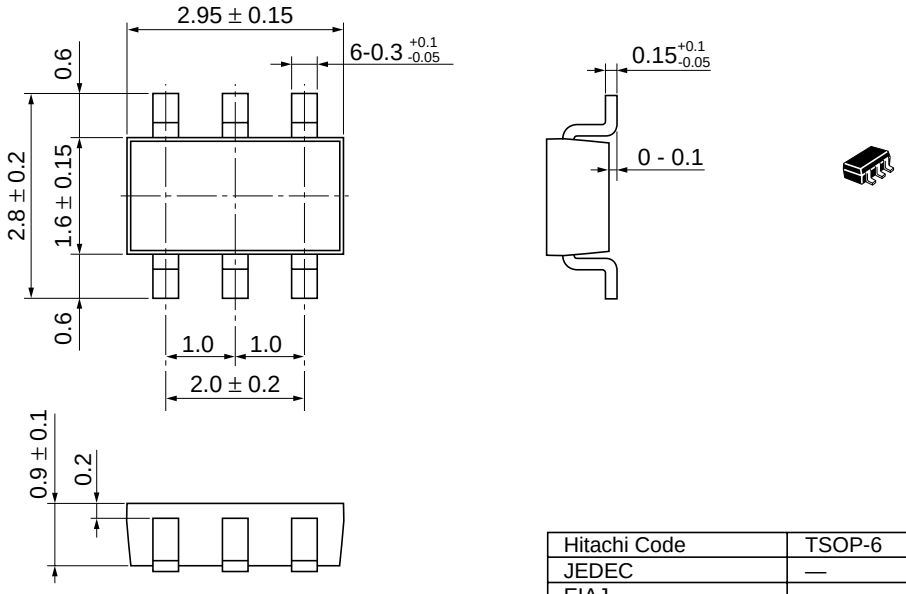



Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
0.0001
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θ ch – f(t) = γs (t) • θch – f
θ ch – f = 119 °C/W, Ta = 25 °C
When using the alumina ceramic board
(50x50x0.7 mm)
PDM
D = PW / T
PW
T
10 µ
100 µ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)

Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	TSOP-6
JEDEC	—
EIAJ	—
Mass (reference value)	0.012 g

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