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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HAT2033R/HAT2033RJ

Silicon N Channel Power MOS FET
High Speed Power Switching

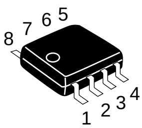
ADE-208-664B (Z)
3rd. Edition
Feb. 1999

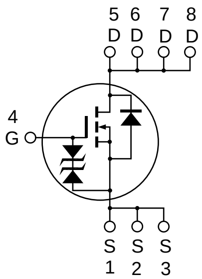
Features

- For Automotive Application (at Type Code “J “)
- Low on-resistance
- Capable of 4 V gate drive
- High density mounting

Outline

SOP–8





1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage		V_{DSS}	60	V
Gate to source voltage		V_{GSS}	± 20	V
Drain current		I_D	7	A
Drain peak current		$I_{D(pulse)}$ Note1	56	A
Body-drain diode reverse drain current		I_{DR}	7	A
Avalanche current	HAT2033R	I_{AP} Note4	—	—
	HAT2033RJ		7	A
Avalanche energy	HAT2033R	E_{AR} Note4	—	—
	HAT2033RJ		4.2	mJ
Channel dissipation		Pch Note2	2.5	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	– 55 to + 150	°C

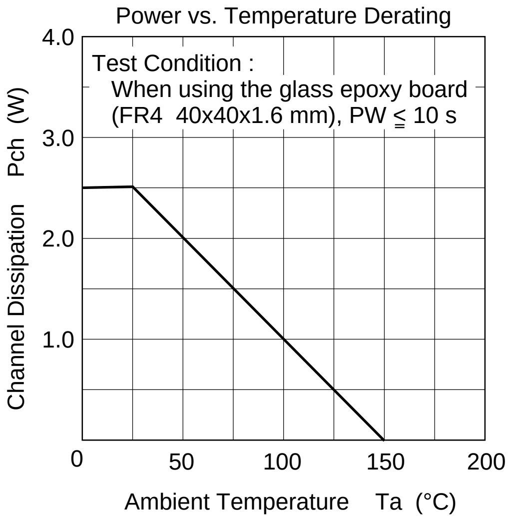
Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW≤ 10s
3. Value at Tch=25°C, Rg≥50Ω

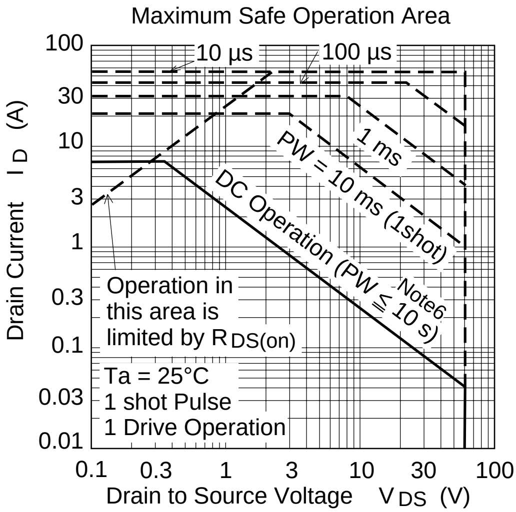
Electrical Characteristics (Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage		$V_{(BR)GSS}$	± 20	—	—	V	I_G = ± 100 μA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	± 10	μA	V_{GS} = ± 16 V, V_{DS} = 0
Zero gate voltage	HAT2033R	I_{DSS}	—	—	1	μA	V_{DS} = 60 V, V_{GS} = 0
drain current	HAT2033RJ	I_{DSS}	—	—	0.1	μA	
Zero gate voltage	HAT2033R	I_{DSS}	—	—	—	μA	V_{DS} =4 8V , V_{GS} = 0
drain current	HAT2033RJ	I_{DSS}	—	—	10	μA	Ta = 125°C
Gate to source cutoff voltage		$V_{GS(off)}$	1.2	—	2.2	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state		$R_{DS(on)}$	—	0.03	0.038	Ω	I_D = 4 A, V_{GS} = 10 V Note4
resistance		$R_{DS(on)}$	—	0.04	0.053	Ω	I_D = 4 A, V_{GS} = 4 V Note4
Forward transfer admittance		$\|y_{fs}\|$	6.5	10	—	S	I_D = 4 A, V_{DS} = 10 V Note4
Input capacitance		Ciss	—	740	—	pF	V_{DS} = 10 V
Output capacitance		Coss	—	370	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	130	—	pF	f = 1MHz
Turn-on delay time		$t_{d(on)}$	—	13	—	ns	V_{GS} =10 V, I_D = 4 A
Rise time		t_r	—	55	—	ns	V_{DD} ≅ 30 V
Turn-off delay time		$t_{d(off)}$	—	140	—	ns	
Fall time		t_f	—	95	—	ns	
Body–drain diode forward voltage		V_{DF}	—	0.82	1.07	V	IF = 7 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time		t_{rr}	—	45	—	ns	IF = 7 A , V_{GS} = 0 diF/ dt = 50 A/μs

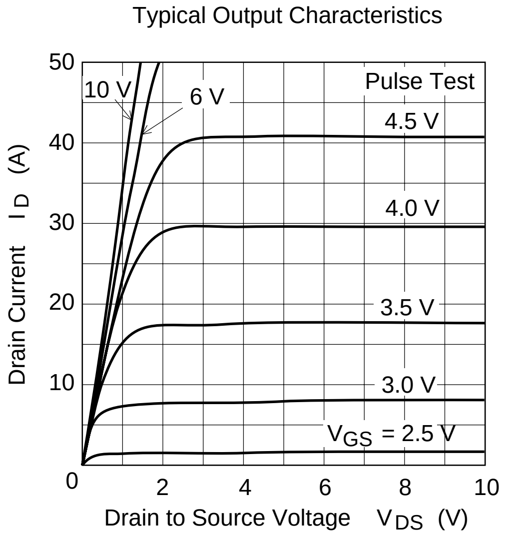
Note: 4. Pulse test

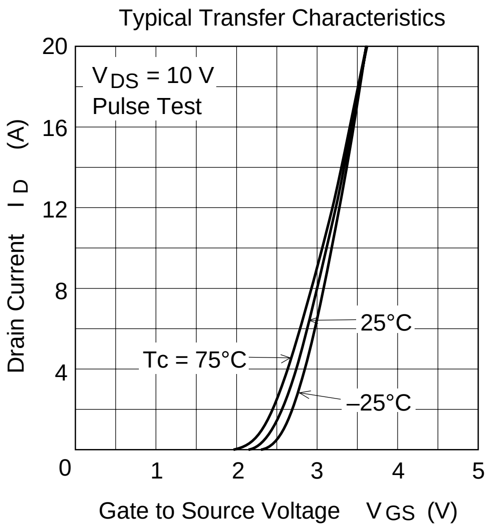
Main Characteristics

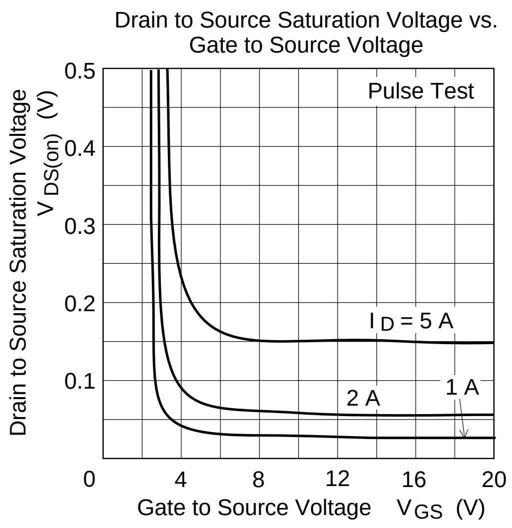


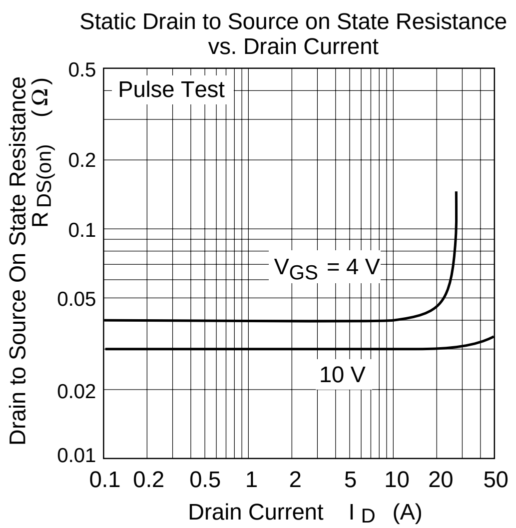


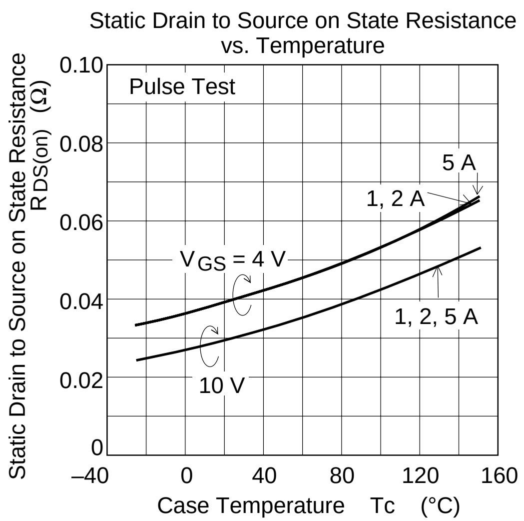
Note 6 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

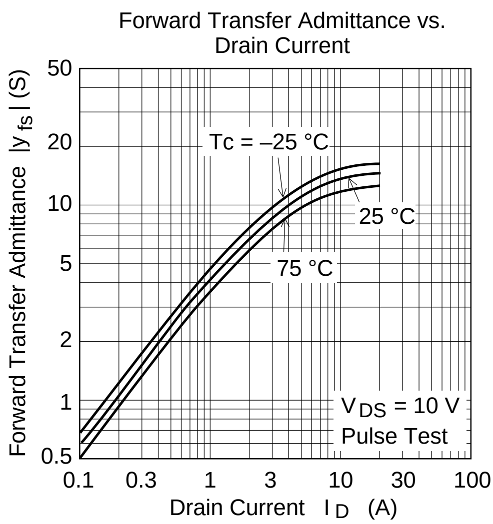


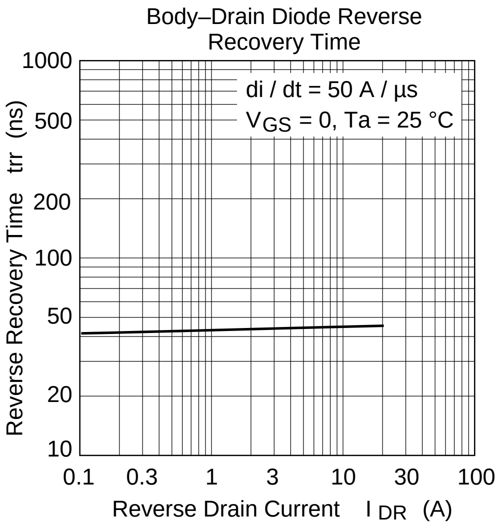


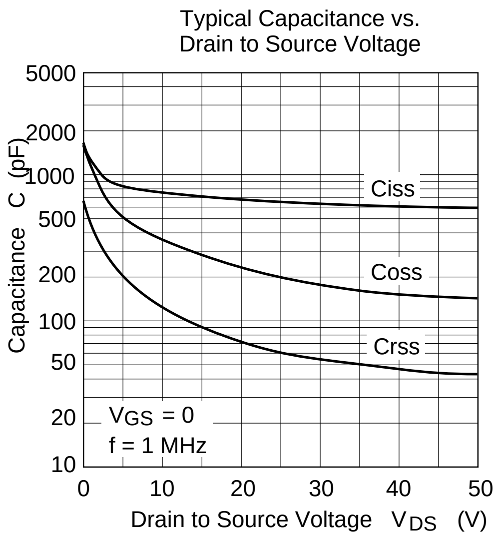

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Saturation Voltage V DS(on) (V)
0.5
0.4
0.3
0.2
0.1
0
4
8
12
16
20
Gate to Source Voltage V GS (V)
Pulse Test
I D = 5 A
2 A
1 A

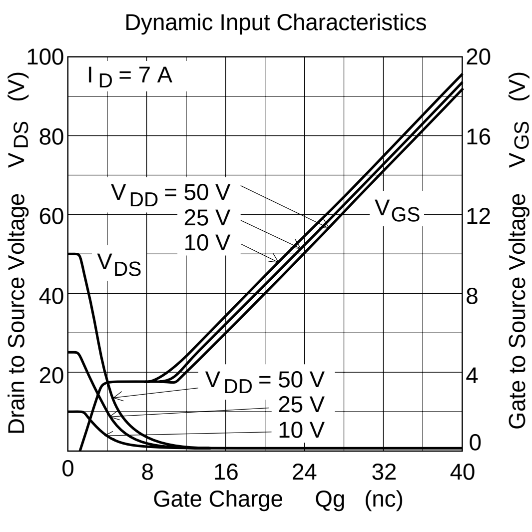

Static Drain to Source on State Resistance
vs. Drain Current
Drain to Source On State Resistance R DS(on) (Ω)
0.5
0.2
0.1
0.05
0.02
0.01
0.1 0.2 0.5 1 2 5 10 20 50
Drain Current I D (A)
Pulse Test
VGS = 4 V
10 V

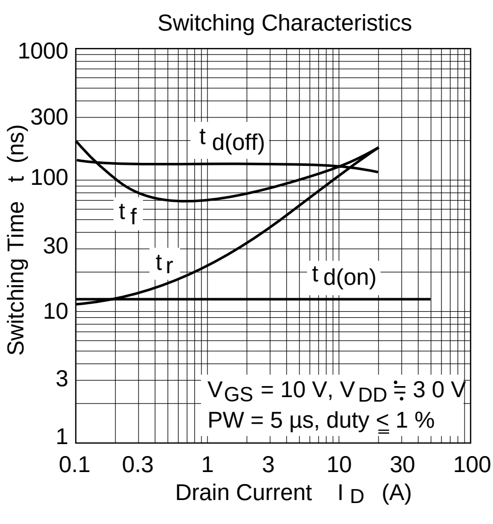

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance R DS(on) (Ω)
0.10
0.08
0.06
0.04
0.02
0
–40
0
40
80
120
160
Case Temperature Tc (°C)
Pulse Test
5 A
1, 2 A
VGS = 4 V
1, 2, 5 A
10 V


Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1
0.5
0.1 0.3 1 3 10 30 100
Drain Current I D (A)
Tc = –25 °C
25 °C
75 °C
VDS = 10 V
Pulse Test

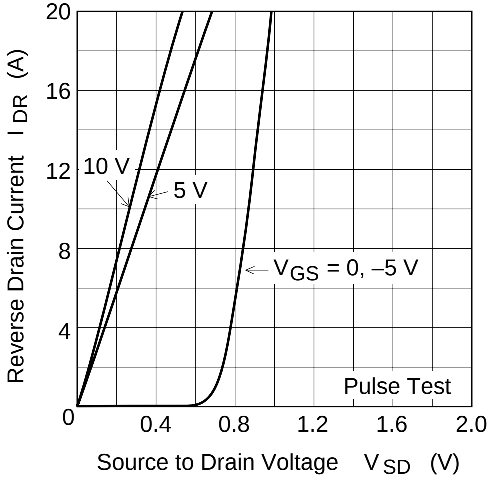

Body–Drain Diode Reverse Recovery Time
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.1
0.3
1
3
10
30
100
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
5000
2000
1000
500
200
100
50
20
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

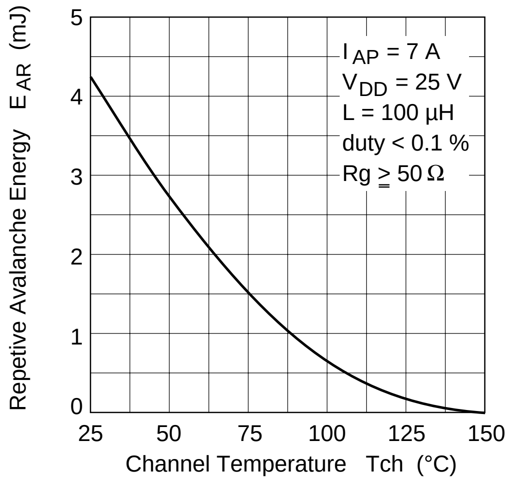

Dynamic Input Characteristics
I D = 7 A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
0
20
16
12
8
4
0
VDD = 50 V
25 V
10 V
VGS
VDS
VDD = 50 V
25 V
10 V
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
300
100
30
10
3
1
t d(off)
t f
t r
t d(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %
0.1
0.3
1
3
10
30
100
Drain Current I D (A)

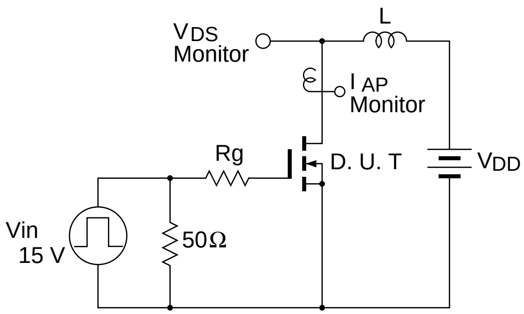
Reverse Drain Current vs.
Souece to Drain Voltage



Maximun Avalanche Energy vs.
Channel Temperature Derating

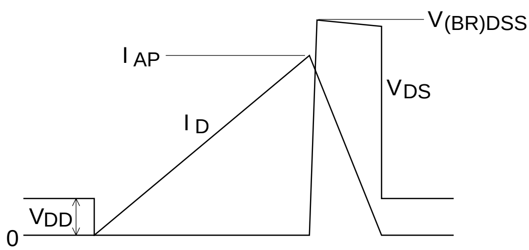


Avalanche Test Circuit

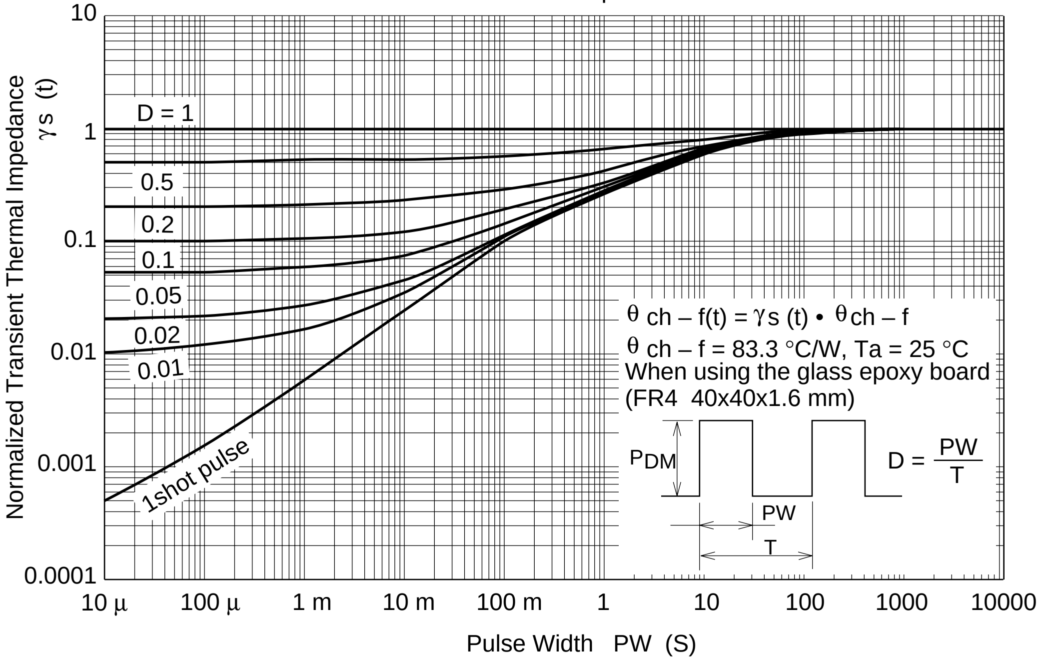


Avalanche Waveform

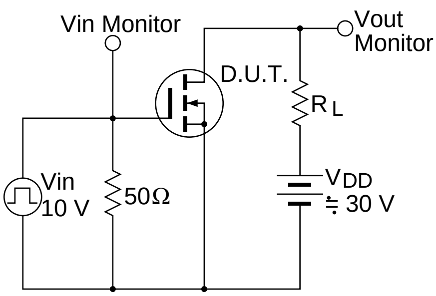
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}{}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



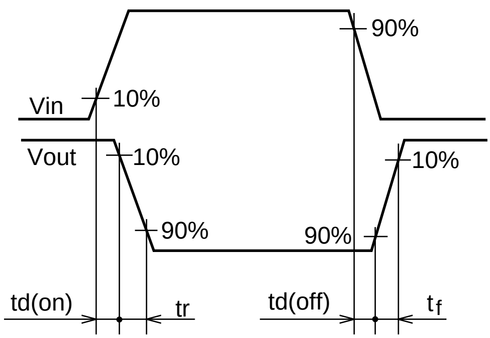
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

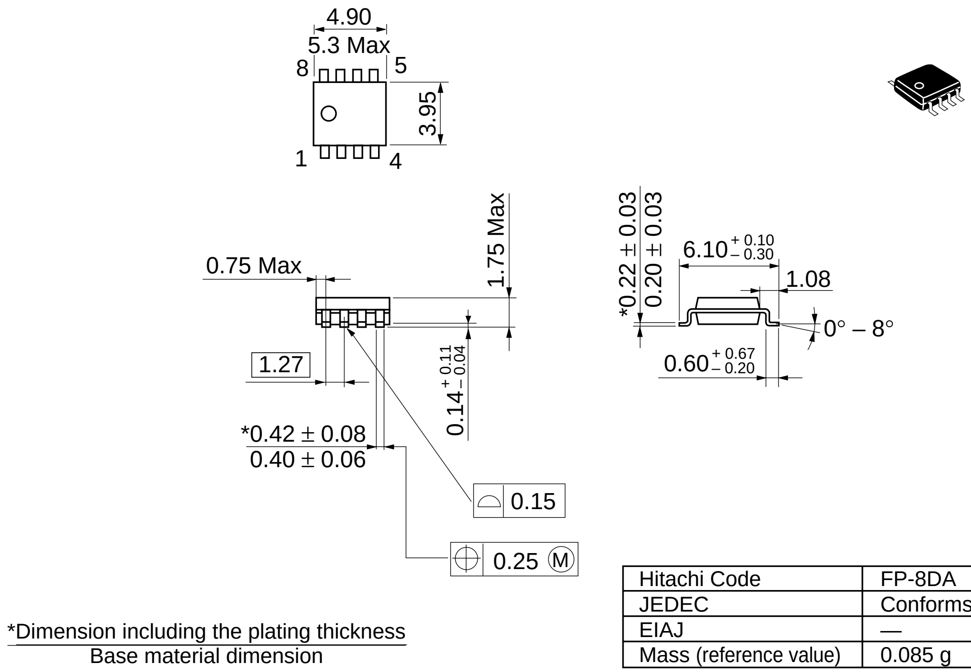


Switching Time Waveform



Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	FP-8DA
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

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Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : http://semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
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For further information write to:

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straβe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : http://www.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
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World Finance Centre,
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