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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HAT2099H

Silicon N Channel Power MOS FET Power Switching

RENESAS

ADE-208-1432C (Z)

4th. Edition
Aug. 2002

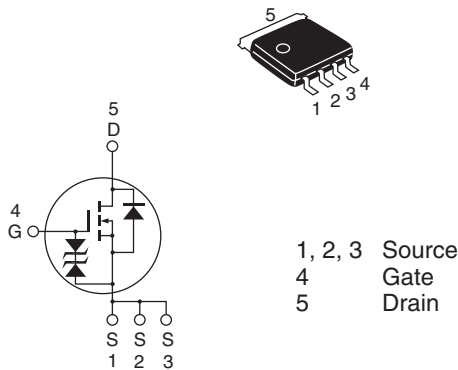
Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance

$$R_{DS(on)} = 2.9 \text{ m}\Omega \text{ typ. (at } V_{GS} = 10 \text{ V)}$$

Outline

LFPAK



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	200	A
Body-drain diode reverse drain current	I_{DR}	50	A
Avalanche current	I_{AP} ^{Note 3}	5	A
Avalanche energy	E_{AR} ^{Note 3}	2.5	mJ
Channel dissipation	P_{ch} ^{Note2}	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to + 150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. $T_c = 25^\circ C$
3. Value at Tch = 25°C, $R_g \geq 50 \Omega$

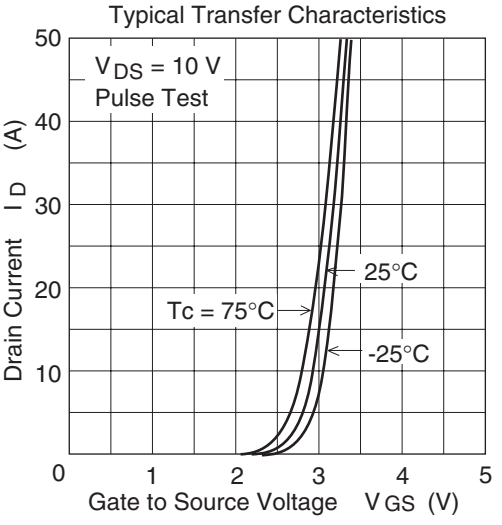
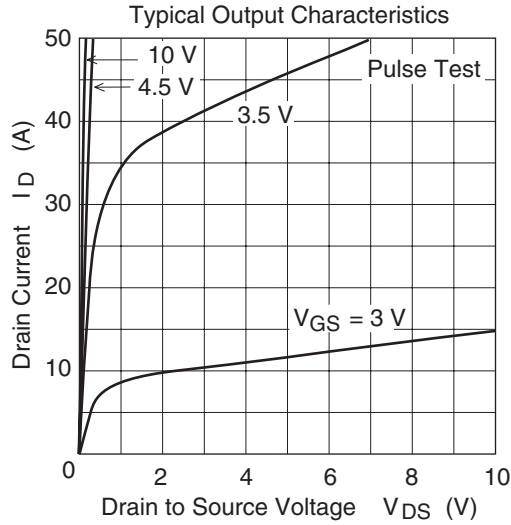
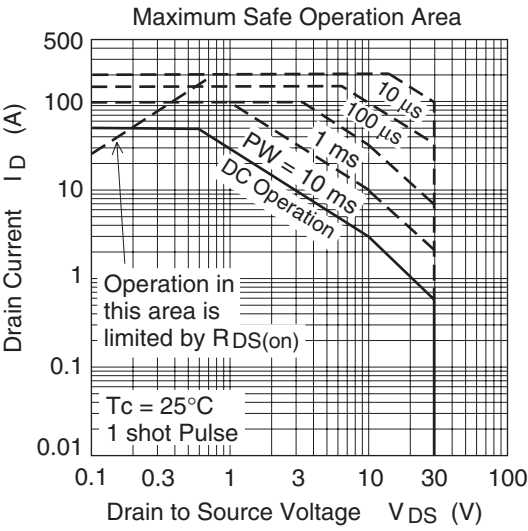
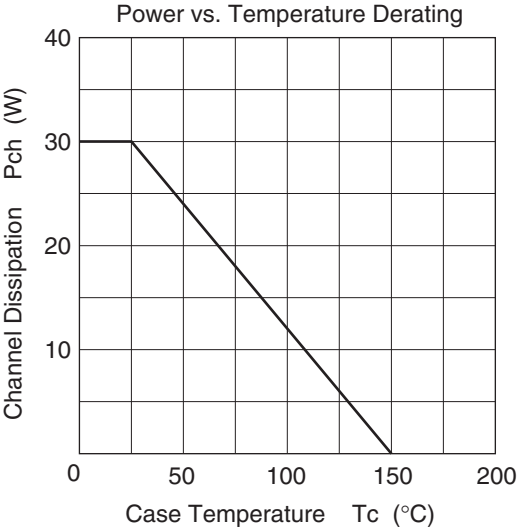
Electrical Characteristics

(Ta = 25°C)

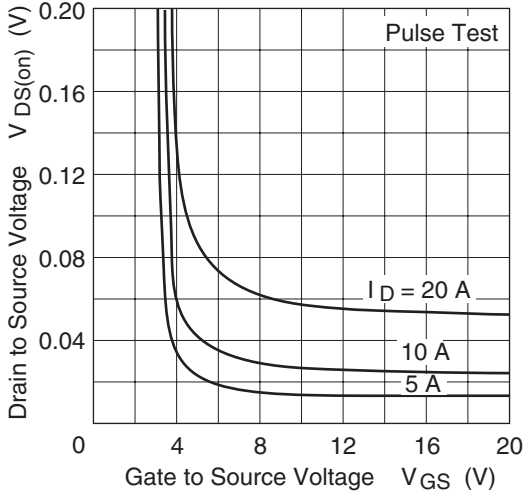
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	2.9	3.7	$\text{m}\Omega$	$I_D = 25 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	5.0	7.3	$\text{m}\Omega$	$I_D = 25 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	39	65	—	S	$I_D = 25 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note3}
Input capacitance	Ciss	—	4750	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	1180	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	650	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Qg	—	75	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Qgs	—	16	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Qgd	—	14	—	nc	$I_D = 50 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	26	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 25 \text{ A}$
Rise time	t_r	—	60	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	$R_L = 0.4 \text{ }\Omega$
Fall time	t_f	—	26	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	0.85	0.98	V	$I_F = 50 \text{ A}$, $V_{GS} = 0$ ^{Note3}
Body-drain diode reverse recovery time	t_{rr}	—	60	—	ns	$I_F = 50 \text{ A}$, $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Notes: 3. Pulse test

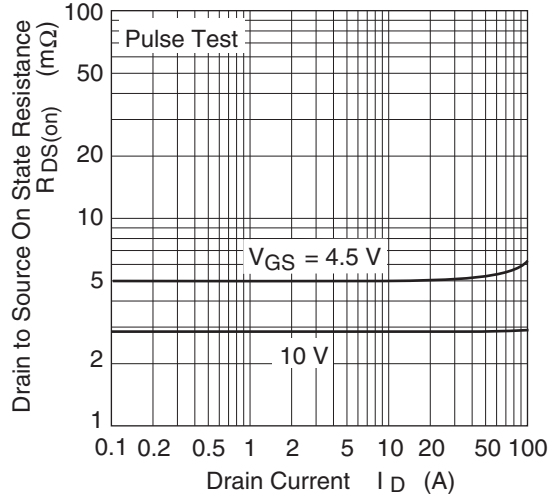
Main Characteristics



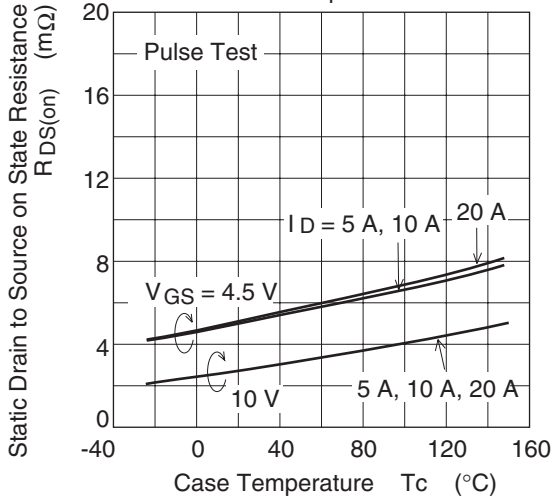
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



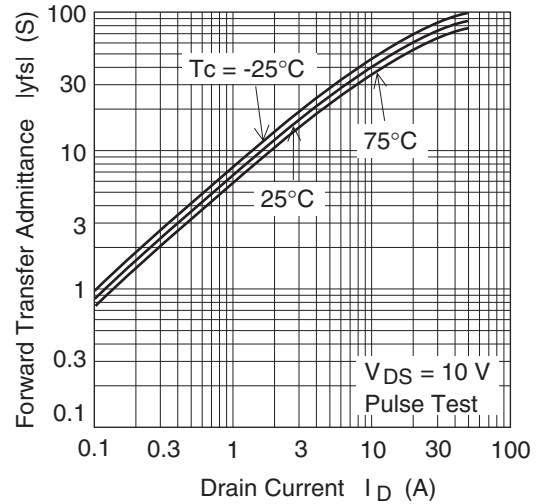
Static Drain to Source on State Resistance
vs. Drain Current



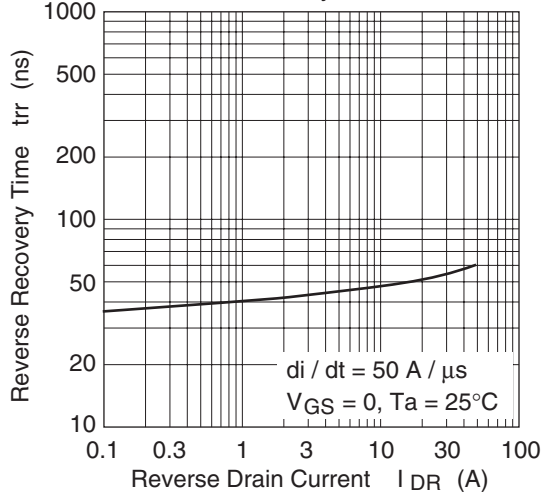
Static Drain to Source on State Resistance
vs. Temperature



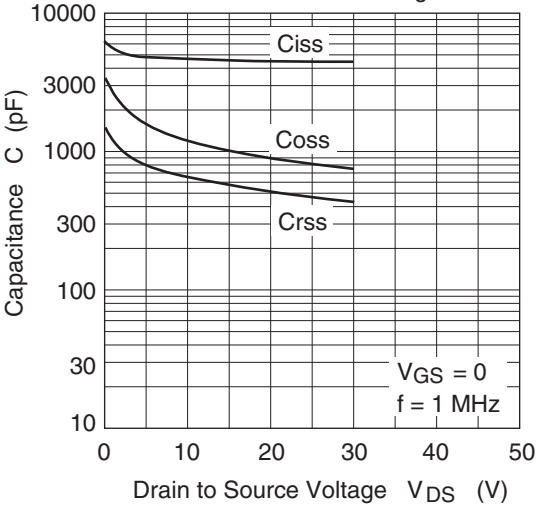
Forward Transfer Admittance vs.
Drain Current



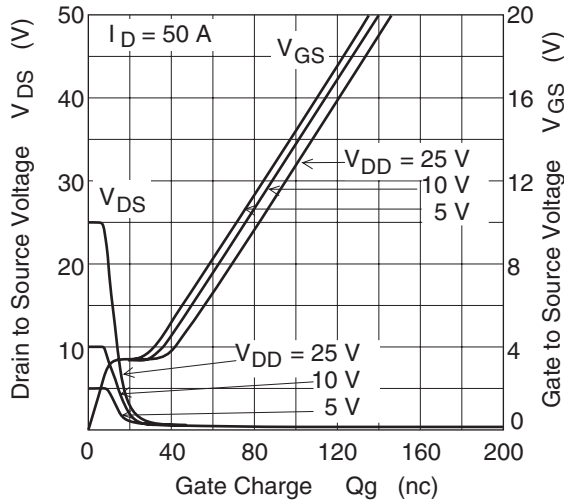
Body-Drain Diode Reverse Recovery Time



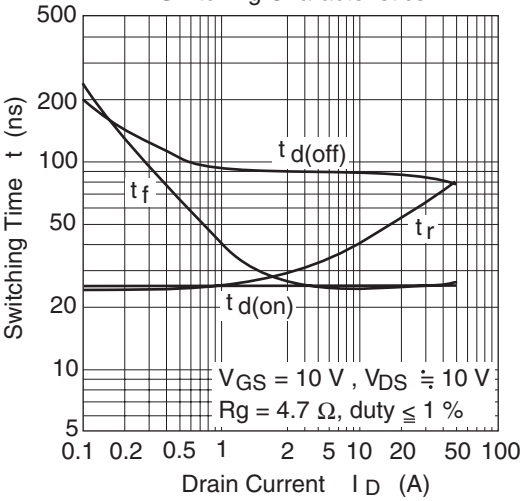
Typical Capacitance vs. Drain to Source Voltage

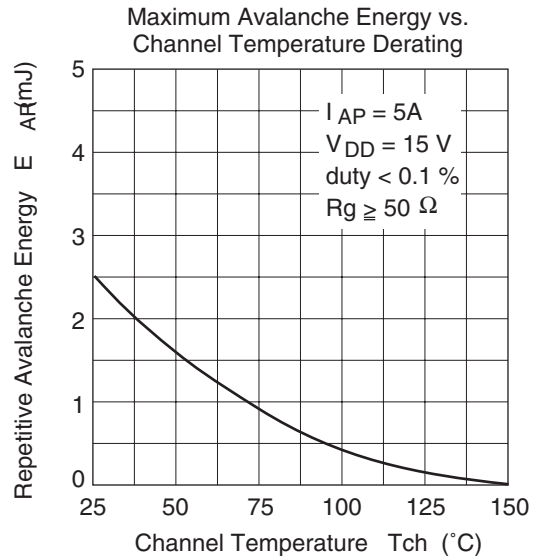
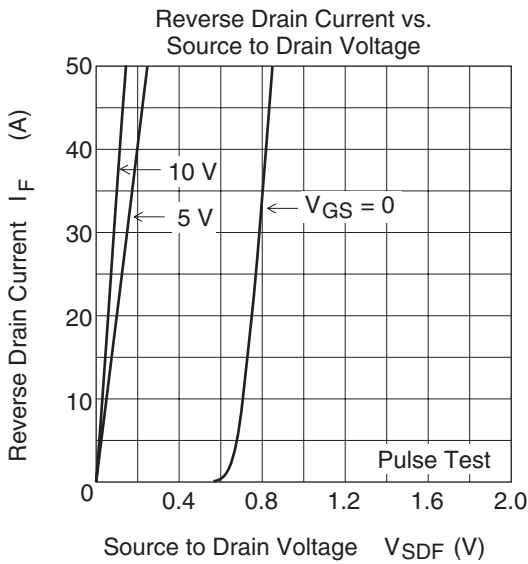


Dynamic Input Characteristics

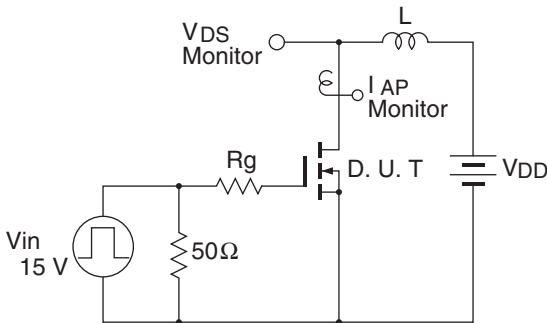


Switching Characteristics



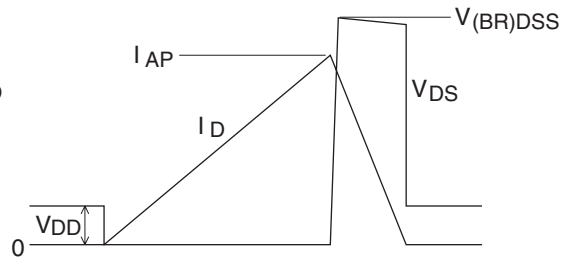


Avalanche Test Circuit

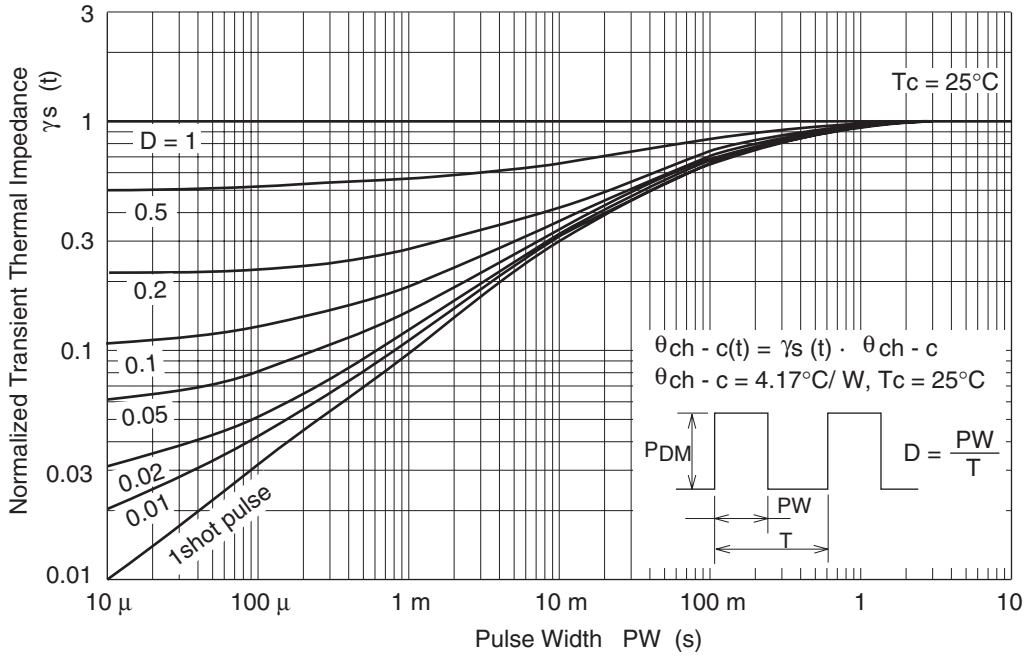


Avalanche Waveform

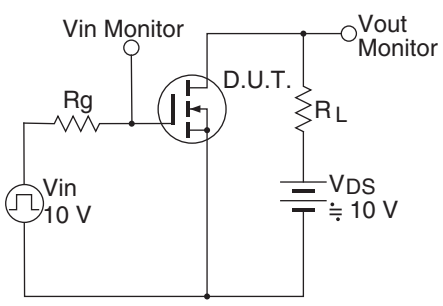
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



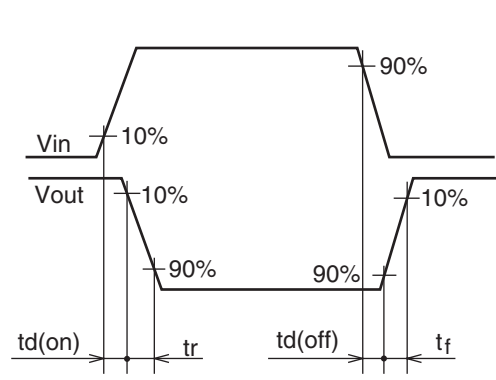
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



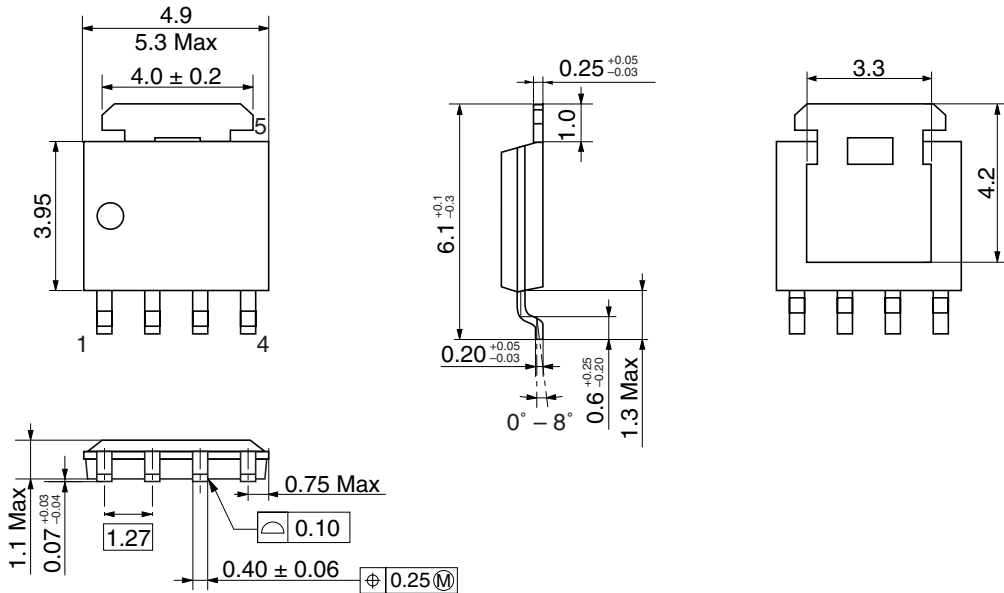
Switching Time Waveform



Package Dimensions

As of January, 2002

Unit: mm



Hitachi Code	LFPK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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