To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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HAT2134H

Silicon N Channel Power MOS FET
Power Switching

ADE-208-1578A (Z)

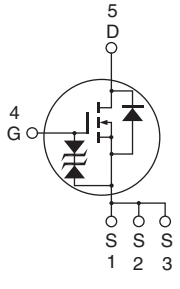
Preliminary
2nd. Edition
Aug. 2002

Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 2.3 mΩ typ. (at V_{GS} = 10 V)

Outline

LFPAK



1, 2, 3	Source
4	Gate
5	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	60	A
Drain peak current	$I_{D(pulse)}$ Note1	240	A
Body-drain diode reverse drain current	I_{DR}	60	A
Avalanche current	I_{AP} Note 3	20	A
Avalanche energy	E_{AR} Note 3	40	mJ
Channel dissipation	Pch Note2	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to + 150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics

(Ta = 25°C)

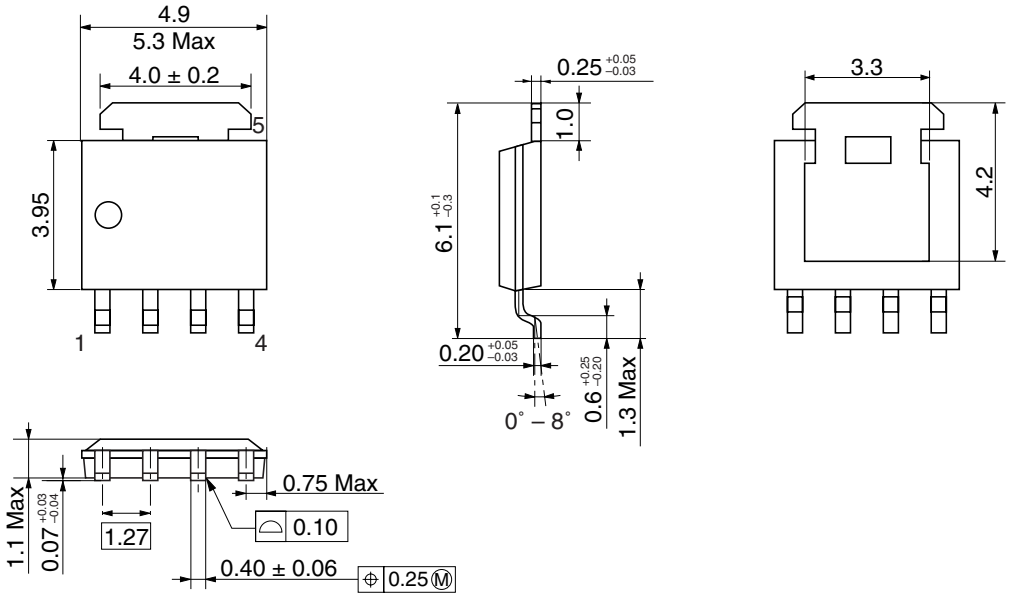
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	2.3	2.9	mΩ	I_D = 30 A, V_{GS} = 10 V [Note4]
	$R_{DS(on)}$	—	4.0	5.8	mΩ	I_D = 30 A, V_{GS} = 4.5 V [Note4]
Forward transfer admittance	$\|y_{fs}\|$	51	85	—	S	I_D = 30 A, V_{DS} = 10 V [Note4]
Input capacitance	Ciss	—	4500	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1200	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	560	—	pF	f = 1 MHz
Total gate charge	Qg	—	70	—	nc	V_{DD} = 10 V
Gate to source charge	Qgs	—	15	—	nc	V_{GS} = 10 V
Gate to drain charge	Qgd	—	11	—	nc	I_D = 60 A
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	V_{GS} = 10 V, I_D = 30 A
Rise time	t_r	—	60	—	ns	V_{DD} ≅ 10 V
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	R_L = 0.33 Ω
Fall time	t_f	—	17	—	ns	Rg = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	0.85	1.10	V	IF = 60 A, V_{GS} = 0 [Note4]
Body–drain diode reverse recovery time	t_{rr}	—	50	—	ns	IF = 60 A, V_{GS} = 0 diF/ dt = 50 A/ µs

Notes: 4. Pulse test

Package Dimensions

As of January, 2002

Unit: mm



Hitachi Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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