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# HD74SSTV16857

## 1:1 14-bit SSTL\_2 Registered Buffer



ADE-205-336F (Z)

Rev.6  
June. 2001

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### Description

The HD74SSTV16857 is a 14-bit registered buffer designed for 2.3 V to 2.7 V V<sub>cc</sub> operation and LVCMOS reset ( $\overline{\text{RESET}}$ ) input / SSTL\_2 data (D) inputs and CLK input.

Data flow from D to Q is controlled by differential clock pins (CLK,  $\overline{\text{CLK}}$ ) and the  $\overline{\text{RESET}}$ . Data is triggered on the positive edge of the positive clock (CLK), and the negative clock ( $\overline{\text{CLK}}$ ) must be used to maintain noise margins. When  $\overline{\text{RESET}}$  is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{\text{RESET}}$  must be held in the low state during power up.

### Features

- Supports LVCMOS reset ( $\overline{\text{RESET}}$ ) input / SSTL\_2 data (D) inputs and CLK input
- Differential SSTL\_2 (Stub series terminated logic) CLK signal
- Flow through architecture optimizes PCB layout
- Package type

| Package type | Package code | Package suffix | Taping code           |
|--------------|--------------|----------------|-----------------------|
| TSSOP-48 pin | TTP-48DB     | T              | EL (1,000 pcs / Reel) |
| TVSOP-48 pin | TTP-48DEV    | N              | EL (1,000 pcs / Reel) |

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**Function Table**

| Inputs                    |                         |        |   | Output Q   |
|---------------------------|-------------------------|--------|---|------------|
| $\overline{\text{RESET}}$ | $\overline{\text{CLK}}$ | CLK    | D |            |
| L                         | X                       | X      | X | L          |
| H                         | ↓                       | ↑      | H | H          |
| H                         | ↓                       | ↑      | L | L          |
| H                         | L or H                  | H or L | X | $Q_0^{*1}$ |

H : High level

L : Low level

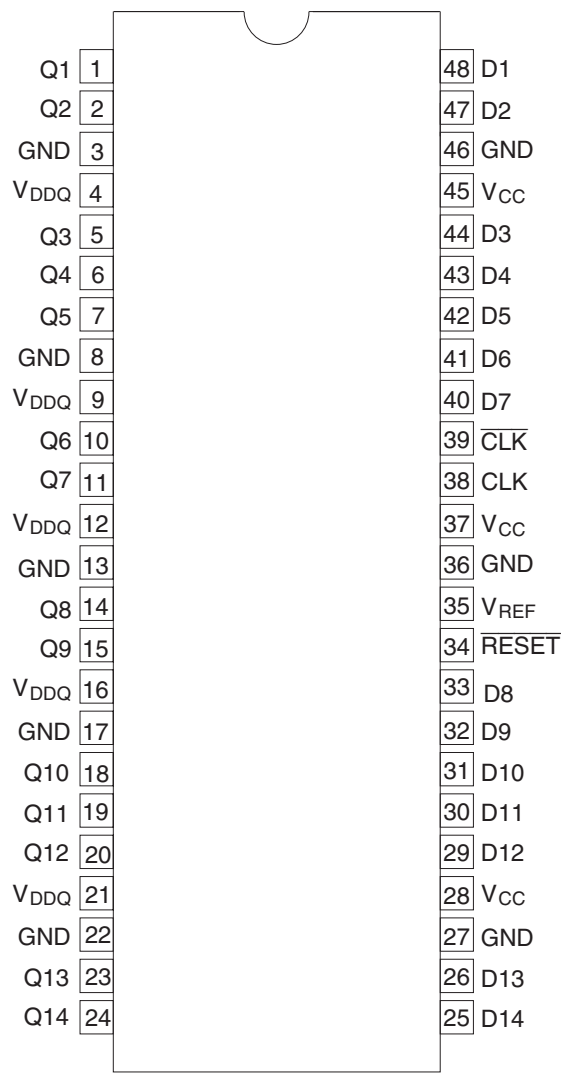
X : Immaterial

↑ : Low to high transition

↓ : High to low transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

## Absolute Maximum Ratings

| Item  | Symbol                            | Ratings               | Unit                        | Conditions                   |
|---|-----------------------------------|-----------------------|-----------------------------|------------------------------|
| Supply voltage  | $V_{CC}$ or $V_{DDQ}$             | -0.5 to 3.6           | V                           |                              |
| Input voltage <sup>1</sup>  | $V_I$                             | -0.5 to $V_{DDQ}+0.5$ | V                           |                              |
| Output voltage <sup>1,2</sup>   | $V_O$                             | -0.5 to $V_{DDQ}+0.5$ | V                           |                              |
| Input clamp current   | $I_{IK}$                          | ±50                   | mA                          | $V_I < 0$ or $V_I > V_{CC}$  |
| Output clamp current  | $I_{OK}$                          | ±50                   | mA                          | $V_O < 0$ or $V_O > V_{DDQ}$ |
| Continuous output current   | $I_O$                             | ±50                   | mA                          | $V_O = 0$ to $V_{DDQ}$       |
| $V_{CC}$ , $V_{DDQ}$ or GND current / pin                               | $I_{CC}$ , $I_{DDQ}$ or $I_{GND}$ | ±100                  | mA                          |                              |
| Maximum power dissipation<br>at $T_a = 55^\circ\text{C}$ (in still air) | $P_T$                             | 115                   | $^\circ\text{C} / \text{W}$ | TSSOP                        |
| Storage temperature   | Tstg                              | -65 to +150           | $^\circ\text{C}$            |                              |

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

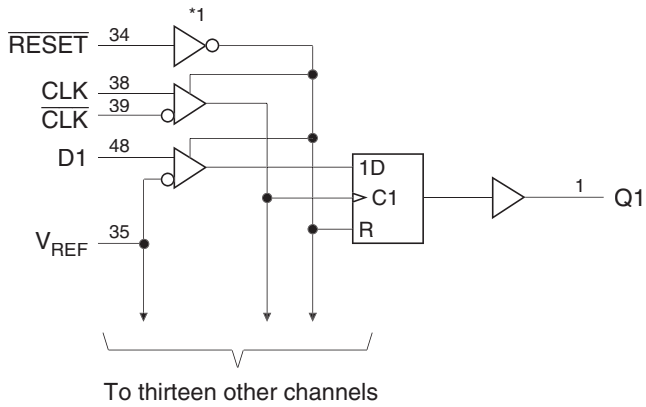
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This current will flow only when the output is in the high state and  $V_O > V_{DDQ}$ .

## Recommended Operating Conditions

| Item                                       | Symbol    | Min                | Typ       | Max                | Unit | Conditions                     |
|--|-----------|--------------------|-----------|--------------------|------|--------------------------------|
| Supply voltage                             | $V_{CC}$  | $V_{DDQ}$          | 2.5       | 2.7                | V    |                                |
| Output supply voltage                      | $V_{DDQ}$ | 2.3                | 2.5       | 2.7                | V    |                                |
| Reference voltage                          | $V_{REF}$ | 1.15               | 1.25      | 1.35               | V    | $V_{REF} = 0.5 \times V_{DDQ}$ |
| Termination voltage                        | $V_{TT}$  | $V_{REF} - 40$ mV  | $V_{REF}$ | $V_{REF} + 40$ mV  | V    |                                |
| Input voltage                              | $V_I$     | 0                  | —         | $V_{CC}$           | V    |                                |
| AC high level input voltage                | $V_{IH}$  | $V_{REF} + 310$ mV | —         | —                  | V    | D                              |
| AC low level input voltage                 | $V_{IL}$  | —                  | —         | $V_{REF} - 310$ mV | V    | D                              |
| DC high level input voltage                | $V_{IH}$  | $V_{REF} + 150$ mV | —         | —                  | V    | D                              |
| DC low level input voltage                 | $V_{IL}$  | —                  | —         | $V_{REF} - 150$ mV | V    | D                              |
| High level input voltage                   | $V_{IH}$  | 1.7                | —         | $V_{DDQ} + 0.3$    | V    | $\overline{\text{RESET}}$      |
| Low level input voltage                    | $V_{IL}$  | -0.3               | —         | 0.7                | V    | $\overline{\text{RESET}}$      |
| Differential (Common mode range)           | $V_{CMR}$ | 0.97               | —         | 1.53               | V    | CLK, $\overline{\text{CLK}}$   |
| input voltage (Minimum peak to peak input) | $V_{PP}$  | 360                | —         | —                  | mV   | CLK, $\overline{\text{CLK}}$   |
| High level output current                  | $I_{OH}$  | —                  | —         | -20                | mA   |                                |
| Low level output current                   | $I_{OL}$  | —                  | —         | 20                 | mA   |                                |
| Operating temperature                      | $T_a$     | 0                  | —         | 70                 | °C   |                                |

Note: The  $\overline{\text{RESET}}$  input of the device must be held at  $V_{DDQ}$  or GND to ensure proper device operation. The differential inputs must not be floating, unless  $\overline{\text{RESET}}$  is low.

## Logic Diagram



Note: 1.  $\overline{\text{RESET}}$  input gate is connected to  $V_{\text{DDQ}}$ .

## Electrical Characteristics

| Item  | Symbol                          | V <sub>CC</sub> (V) | Min                  | Typ | Max              | Unit  | Test Conditions   |  |
|---|---------------------------------|---------------------|----------------------|-----|------------------|---|---|--|
| Input diode voltage   | V <sub>IK</sub>                 | 2.3                 | —                    | —   | -1.2             | V   | I <sub>IN</sub> = -18 mA  |  |
| Output voltage  | V <sub>OH</sub>                 | 2.3 to 2.7          | V <sub>CC</sub> -0.2 | —   | —                | V   | I <sub>OH</sub> = -100 μA   |  |
|   |                                 | 2.3                 | 1.95                 | —   | V <sub>DDQ</sub> |   | I <sub>OH</sub> = -16 mA  |  |
|   | V <sub>OL</sub>                 | 2.3 to 2.7          | —                    | —   | 0.2              |   | I <sub>OL</sub> = 100 μA  |  |
|   |                                 | 2.3                 | 0                    | —   | 0.35             |   | I <sub>OL</sub> = 16 mA   |  |
| Input current (All inputs)  | I <sub>IN</sub>                 | 2.7                 | —                    | —   | ±5               | μA  | V <sub>IN</sub> = 2.7 V or 0  |  |
| Quiescent supply current  | I <sub>CC</sub> <sup>*2</sup>   | 2.7                 | —                    | —   | 45               | mA  | V <sub>IN</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , I <sub>O</sub> = 0   |  |
| Standby current   | I <sub>CC (stdy)</sub>          | 2.7                 | —                    | —   | 10               | μA  | $\overline{\text{RESET}}$ = GND   |  |
| Dynamic operating clock only  | I <sub>CCD</sub> <sup>*2</sup>  | 2.7                 | —                    | —   | 90               | μA/<br>MHz  | $\overline{\text{RESET}}$ = V <sub>CC</sub> ,<br>clock V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> ,<br>CLK and $\overline{\text{CLK}}$ switching 50%<br>duty cycle   |  |
| Dynamic operating per each data input                               | I <sub>CCD</sub> <sup>*2</sup>  | 2.7                 | —                    | —   | 15               | μA/<br>MHz  | $\overline{\text{RESET}}$ = V <sub>CC</sub> ,<br>clock V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> ,<br>CLK and $\overline{\text{CLK}}$ switching 50%<br>/ duty cycle. One data input<br>data switching at half clock<br>input frequency, 50% duty cycle. |  |
| Output high <sup>*3</sup>   | r <sub>OH</sub>                 | 2.3 to 2.7          | 7                    | —   | 22 <sup>*4</sup> | Ω   | I <sub>OH</sub> = -20 mA  |  |
| Output low <sup>*3</sup>  | r <sub>OL</sub>                 | 2.3 to 2.7          | 7                    | —   | 22 <sup>*4</sup> | Ω   | I <sub>OL</sub> = 20 mA   |  |
| r <sub>OH</sub> - r <sub>OL</sub>   each separate bit <sup>*3</sup> | r <sub>O(Δ)</sub>               | 2.5                 | —                    | —   | 4                | Ω   | I <sub>O</sub> = 20 mA, Ta = 25°C   |  |
| Input capacitance   | Data inputs                     | C <sub>IN</sub>     | 2.5 <sup>*1</sup>    | 2.5 | —                | 3.5   | pF  | V <sub>I</sub> = V <sub>REF</sub> ± 310 mV |
|   | CLK and $\overline{\text{CLK}}$ |                     | 2.5                  | —   | 3.5              | V <sub>CMR</sub> = 1.25 V, V <sub>PP</sub> = 360 mV |   |  |
|   | $\overline{\text{RESET}}$       |                     | —                    | 3.0 | —                | V <sub>I</sub> = V <sub>CC</sub> or GND             |   |  |

Notes: 1. All typical values are at V<sub>CC</sub> = 2.5 V, Ta = 25°C.

2. Total I<sub>CC</sub> (max) = I<sub>CC</sub> + {I<sub>CCD</sub> (clock) × f(clock)} + {I<sub>CCD</sub> (Data) × 1/2f(clock) × 14}

3. This is effective in the case that it did terminate by resistance.

4. See figure. 1, 2

## Switching Characteristics

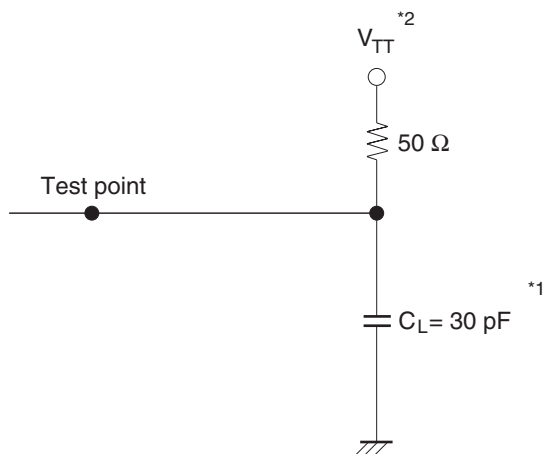
| Item                              | Symbol                          | $V_{CC} = 2.5 \pm 0.2 \text{ V}$ |      | Unit    | Test Condition   |   |
|-----------------------------------|---------------------------------|----------------------------------|------|---------|--|---|
|                                   |                                 | Min                              | Max  |         |  |   |
| Clock frequency <sup>*1</sup>     | $f_{\text{clock}}$              | —                                | 200  | MHz     |  |   |
| Setup time                        | Fast slew rate <sup>*4, 6</sup> | $t_{\text{su}}$                  | 0.75 | —       | ns   | Data before $\text{CLK}\uparrow, \overline{\text{CLK}}\downarrow$ |
|                                   | Slow slew rate <sup>*5, 6</sup> |                                  | 0.9  | —       |  |   |
| Hold time                         | Fast slew rate <sup>*4, 6</sup> | $t_{\text{h}}$                   | 0.75 | —       | ns   | Data after $\text{CLK}\uparrow, \overline{\text{CLK}}\downarrow$  |
|                                   | Slow slew rate <sup>*5, 6</sup> |                                  | 0.9  | —       |  |   |
| Differential inputs active time   | $t_{\text{act}}$                | 22                               | —    | ns      | Data inputs must be low after $\overline{\text{RESET}}$ high.  |   |
| Differential inputs inactive time | $t_{\text{inact}}$              | 22                               | —    | ns      | Data and clock inputs must be held at valid levels (not floating) after $\overline{\text{RESET}}$ low. |   |
| Pulse width                       | $t_{\text{w}}$                  | 2.5                              | —    | ns      | $\text{CLK}, \overline{\text{CLK}}$ "H" or "L"   |   |
| Output slew <sup>*3</sup>         | $t_{\text{SL}}$                 | 1                                | 4    | volt/ns |  |   |

$$(C_L = 30 \text{ pF}, R_L = 50 \Omega, V_{\text{REF}} = V_{\text{TT}} = V_{\text{DDQ}} \times 0.5)$$

| Item                                 | Symbol                           | $V_{CC} = 2.5 \pm 0.2 \text{ V}$ |     |     | Unit | FROM (Input)                        | TO (Output)               |
|--------------------------------------|----------------------------------|----------------------------------|-----|-----|------|-------------------------------------|---------------------------|
|                                      |                                  | Min                              | Typ | Max |      |                                     |                           |
| Maximum clock frequency              | $f_{\text{max}}$                 | 200                              | —   | —   | MHz  |                                     |                           |
| Propagation delay time <sup>*2</sup> | $t_{\text{PLH}}, t_{\text{PHL}}$ | 1.1                              | —   | 2.8 | ns   | $\text{CLK}, \overline{\text{CLK}}$ | Q                         |
|                                      | $t_{\text{PHL}}$                 | —                                | —   | 5.0 |      |                                     | $\overline{\text{RESET}}$ |

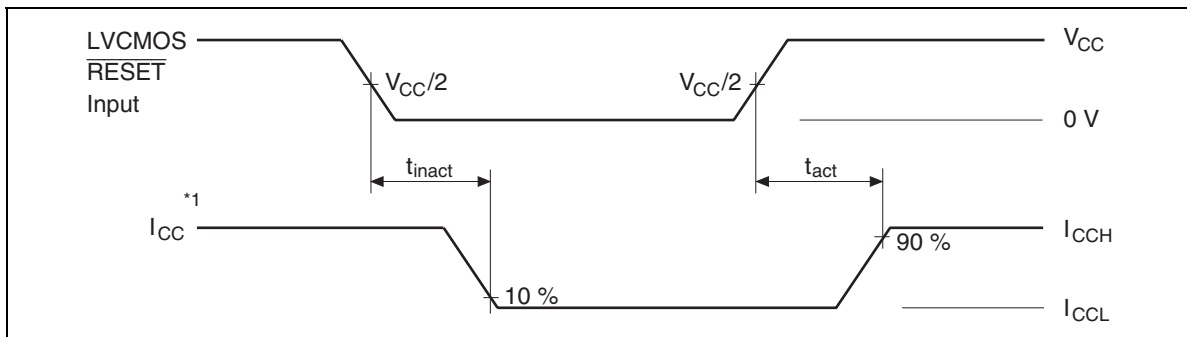
- Notes:
1. Although the clock is differential, all timing is relative to  $\text{CLK}$  going high and  $\overline{\text{CLK}}$  going low.
  2. This timing relationship is specified into test load (see waveforms – 3, 4) with all of the outputs switching.
  3. Assumes into an equivalent, distributed load to the address net structure defined in the application information provided in this specification.
  4. For data signal input slew rate  $\geq 1 \text{ V/ns}$ .
  5. For data signal input slew rate  $\geq 0.5 \text{ V/ns}$  and  $< 1 \text{ V/ns}$ .
  6.  $\text{CLK}, \overline{\text{CLK}}$  signals input slew rates are  $\geq 1 \text{ V/ns}$ .

Test Circuit

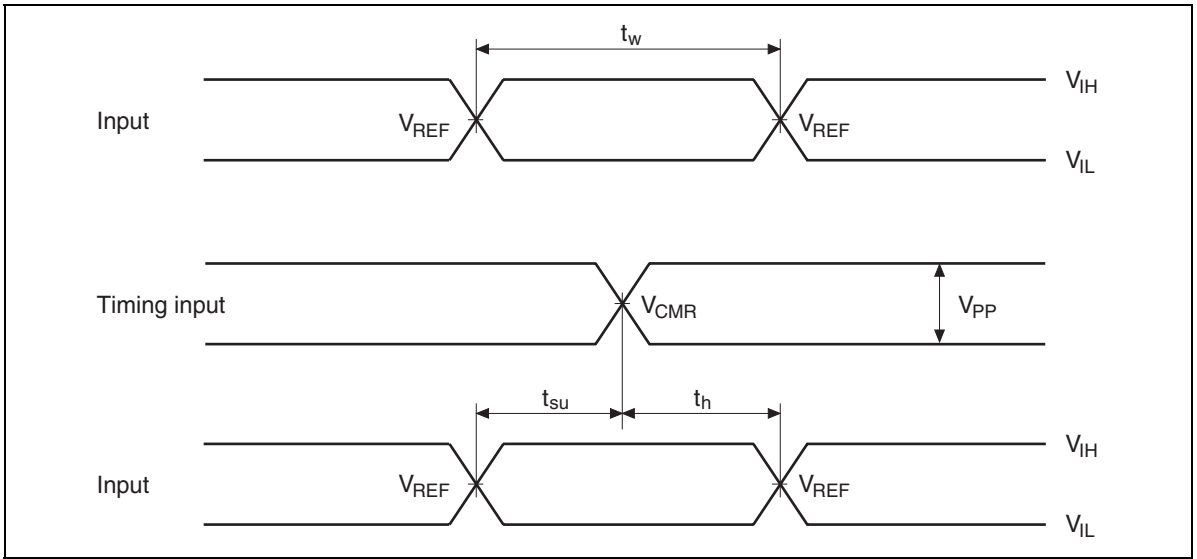


- Notes:
1.  $C_L$  includes probe and jig capacitance.
  2.  $V_{TT} = V_{REF} = V_{DDQ} \times 0.5$

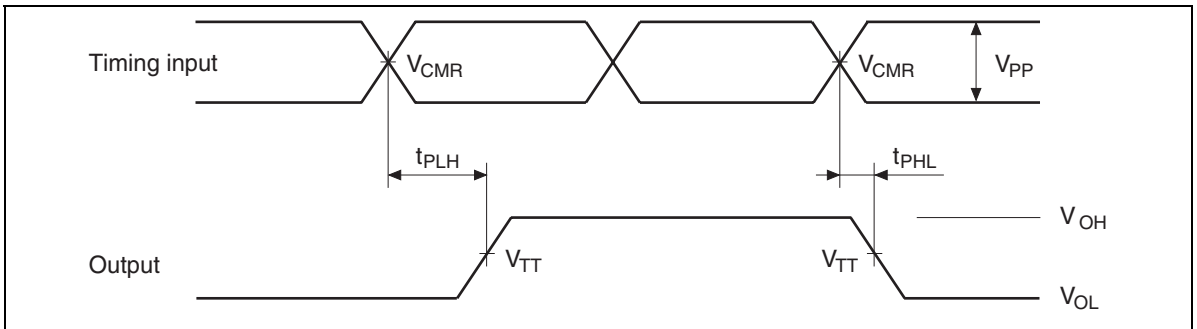
Waveforms - 1



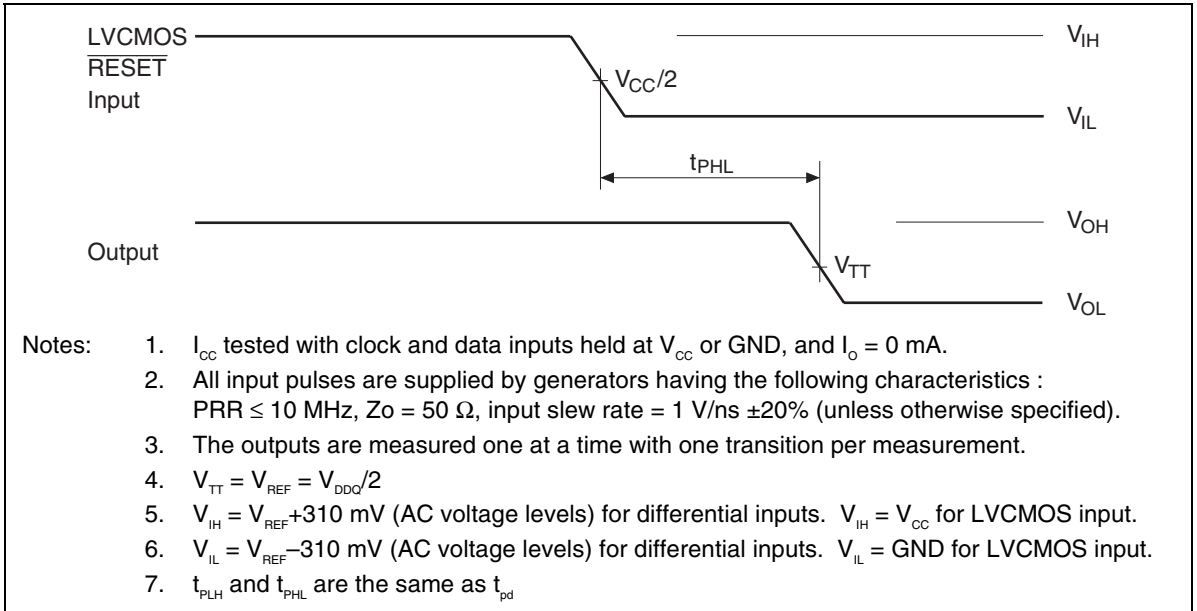
## Waveforms – 2



## Waveforms – 3



Waveforms – 4



## Application Data

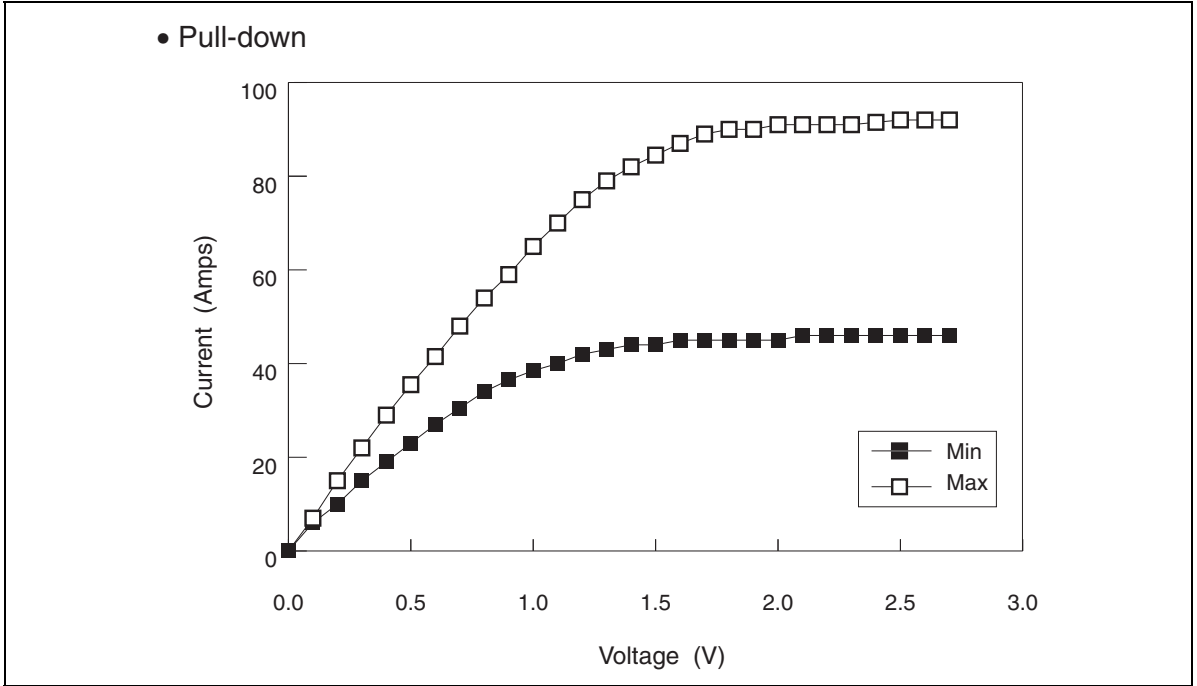


Figure . 1

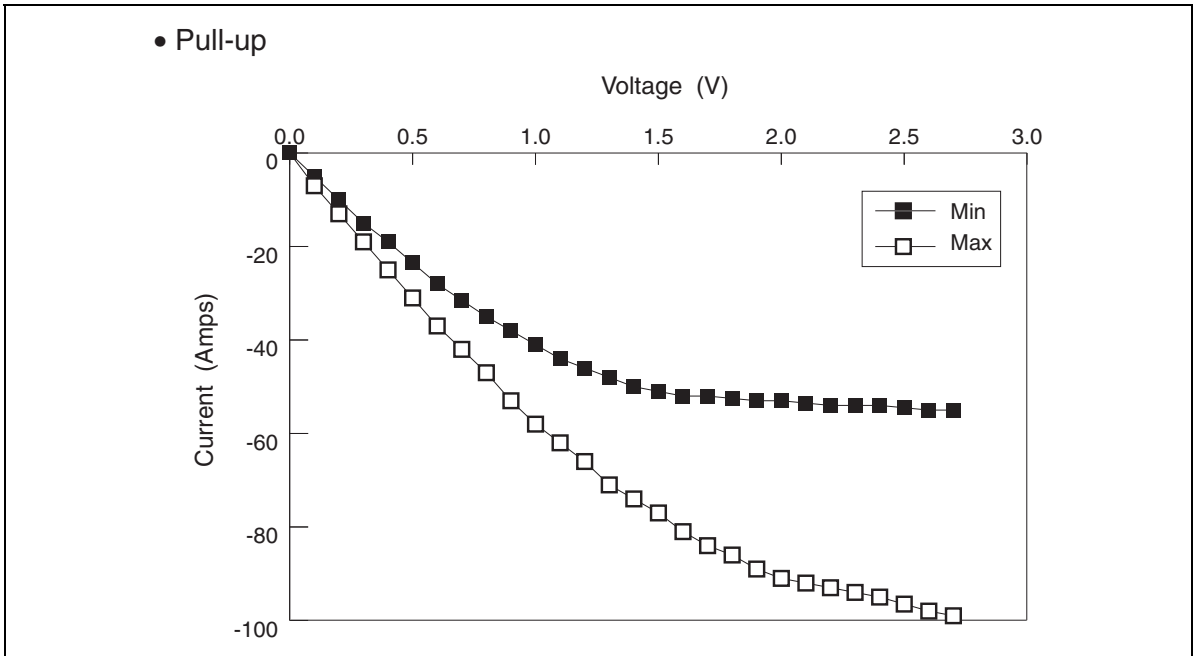


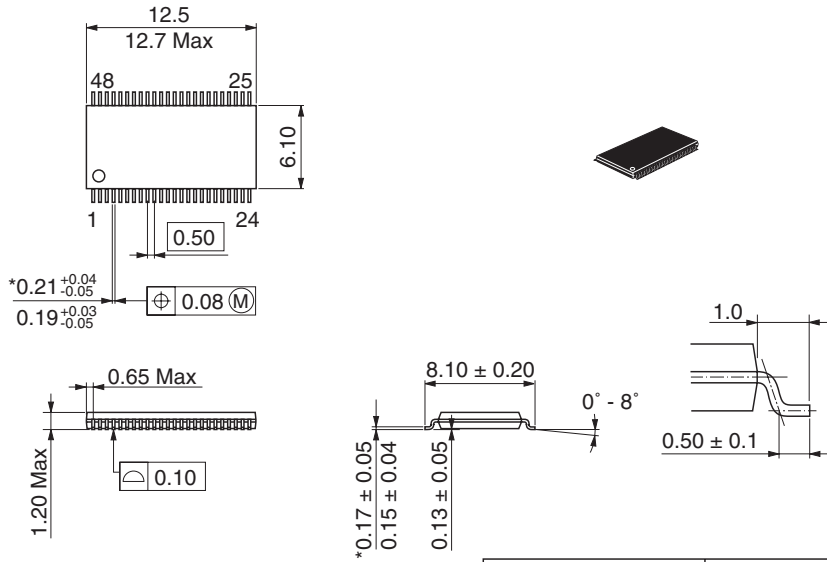
Figure . 2

## Curve Data

| Voltage (V) | Pull-down |        | Pull-up |        |
|-------------|-----------|--------|---------|--------|
|             | I (mA)    | I (mA) | I (mA)  | I (mA) |
|             | Min       | Max    | Min     | Max    |
| 0.0         | 0         | 0      | 0       | 0      |
| 0.1         | 6         | 7      | -5      | -7     |
| 0.2         | 10        | 15     | -10     | -13    |
| 0.3         | 15        | 22     | -15     | -19    |
| 0.4         | 19        | 29     | -19     | -25    |
| 0.5         | 23        | 35.5   | -23.5   | -31    |
| 0.6         | 27        | 41.5   | -28     | -37    |
| 0.7         | 30.5      | 48     | -31.5   | -42    |
| 0.8         | 34        | 54     | -35     | -47    |
| 0.9         | 36.5      | 59     | -38     | -53    |
| 1.0         | 38.5      | 65     | -41     | -58    |
| 1.1         | 40        | 70     | -44     | -62    |
| 1.2         | 42        | 75     | -46     | -66    |
| 1.3         | 43        | 79     | -48     | -71    |
| 1.4         | 44        | 82     | -50     | -74    |
| 1.5         | 44        | 84.5   | -51     | -77    |
| 1.6         | 45        | 87     | -52     | -81    |
| 1.7         | 45        | 89     | -52     | -84    |
| 1.8         | 45        | 90     | -52.5   | -86    |
| 1.9         | 45        | 90     | -53     | -89    |
| 2.0         | 45        | 91     | -53     | -91    |
| 2.1         | 46        | 91     | -53.5   | -92    |
| 2.2         | 46        | 91     | -54     | -93    |
| 2.3         | 46        | 91     | -54     | -94    |
| 2.4         | 46        | 91.5   | -54     | -95    |
| 2.5         | 46        | 92     | -54.5   | -96.5  |
| 2.6         | 46        | 92     | -55     | -98    |
| 2.7         | 46        | 92     | -55     | -99    |

## Package Dimensions

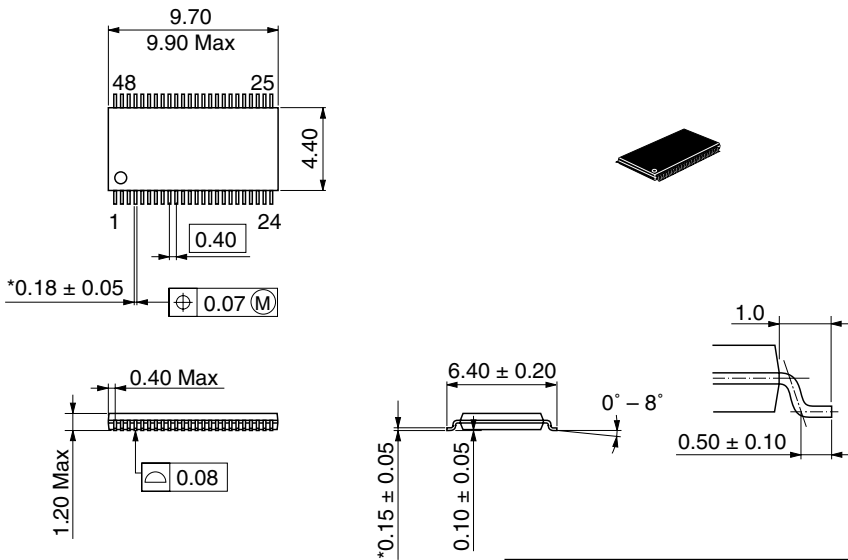
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

|                        |          |
|------------------------|----------|
| Hitachi Code           | TTP-48DB |
| JEDEC                  | —        |
| EIAJ                   | —        |
| Mass (reference value) | 0.20 g   |

Unit: mm



\*Pd plating

|                        |           |
|------------------------|-----------|
| Hitachi Code           | TTP-48DEV |
| JEDEC                  | —         |
| JEITA                  | —         |
| Mass (reference value) | —         |

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