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Customer Support Dept.  
April 1, 2003

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# HM62V16256CI Series

Wide Temperature Range Version  
4 M SRAM (256-kword × 16-bit)



ADE-203-1230C (Z)  
Rev. 3.0  
Jul. 23, 2001

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## Description

The Hitachi HM62V16256CI Series is 4-Mbit static RAM organized 262,144-word × 16-bit. HM62V16256CI Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in standard 44-pin plastic TSOPII.

## Features

- Single 2.5 V and 3.0 V supply: 2.2 V to 3.6 V
- Fast access time: 70 ns (max)
- Power dissipation:
  - Active: 5.0 mW/MHz (typ) ( $V_{CC} = 2.5$  V)  
: 6.0 mW/MHz (typ) ( $V_{CC} = 3.0$  V)
  - Standby: 2  $\mu$ W (typ) ( $V_{CC} = 2.5$  V)  
: 2.4  $\mu$ W (typ) ( $V_{CC} = 3.0$  V)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range:  $-40$  to  $+85^{\circ}\text{C}$

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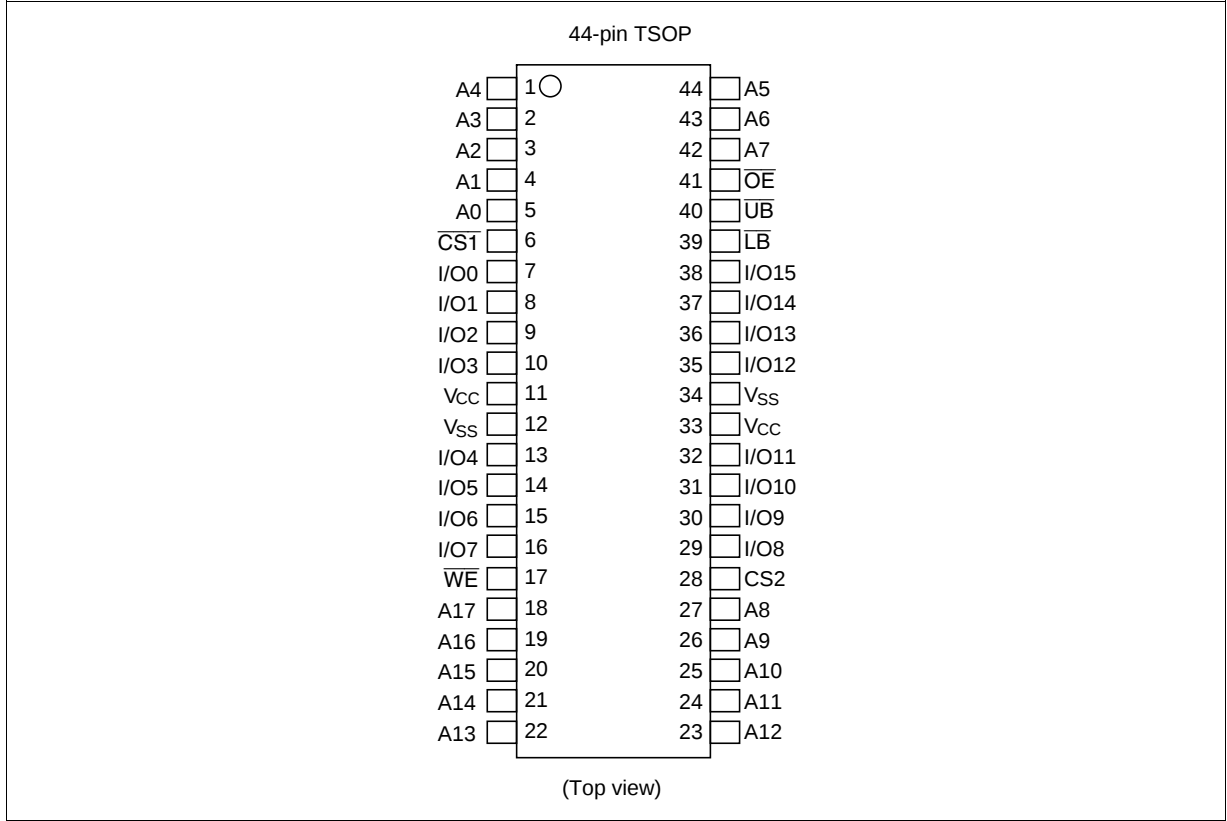
# HM62V16256CI Series

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## Ordering Information

| Type No.          | Access time | Package                                                     |
|-------------------|-------------|-------------------------------------------------------------|
| HM62V16256CLTTI-7 | 70 ns       | 400-mil 44-pin plastic TSOPII (normal-bend type) (TTP-44DB) |

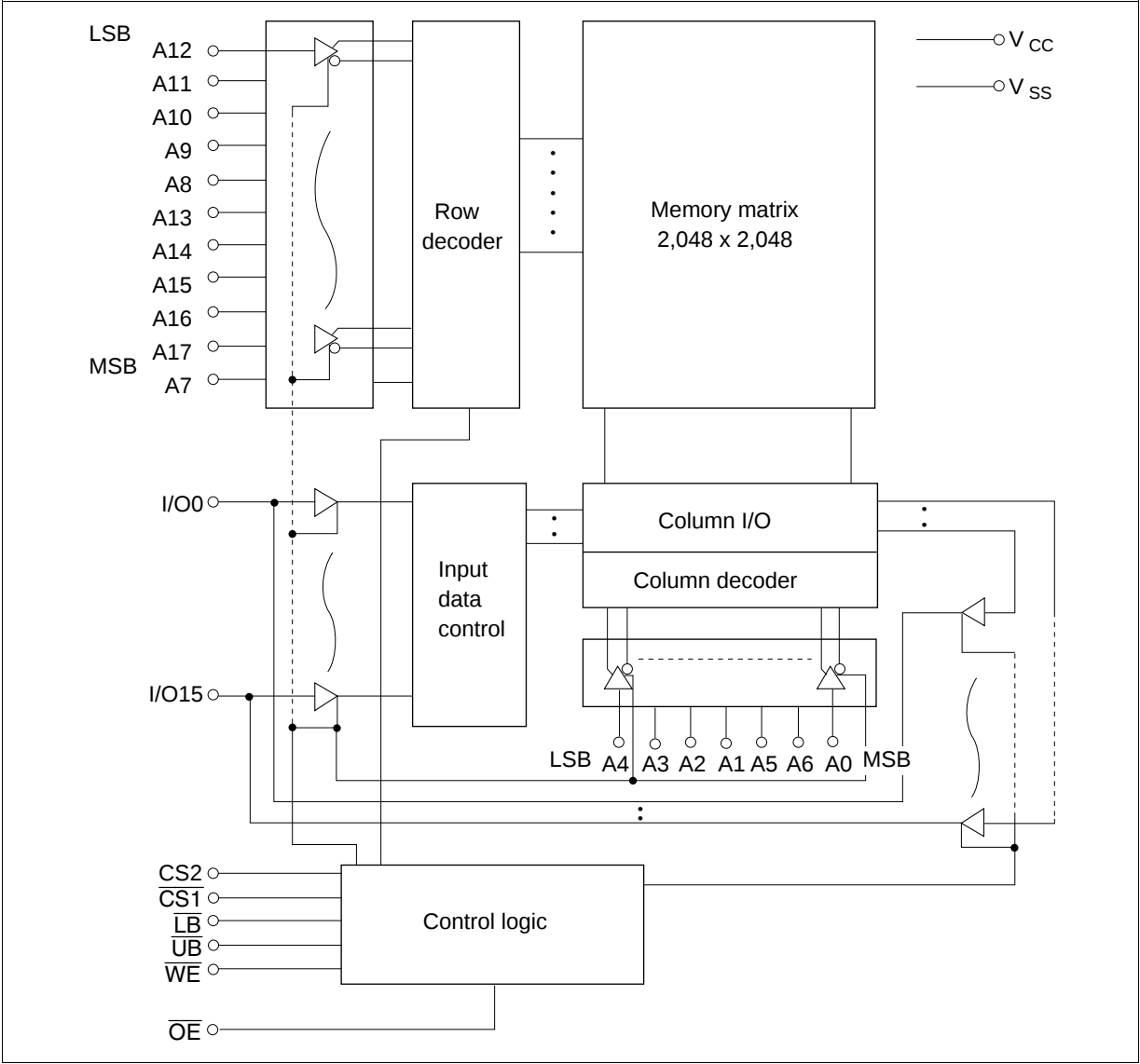
Pin Arrangement



Pin Description

| Pin name                | Function          |
|-------------------------|-------------------|
| A0 to A17               | Address input     |
| I/O0 to I/O15           | Data input/output |
| $\overline{\text{CS1}}$ | Chip select 1     |
| CS2                     | Chip select 2     |
| $\overline{\text{WE}}$  | Write enable      |
| $\overline{\text{OE}}$  | Output enable     |
| $\overline{\text{LB}}$  | Lower byte select |
| $\overline{\text{UB}}$  | Upper byte select |
| V <sub>cc</sub>         | Power supply      |
| V <sub>ss</sub>         | Ground            |

Block Diagram



## Operation Table

| $\overline{CS1}$ | CS2 | $\overline{WE}$ | $\overline{OE}$ | $\overline{UB}$ | $\overline{LB}$ | I/O0 to I/O7 | I/O8 to I/O15 | Operation        |
|------------------|-----|-----------------|-----------------|-----------------|-----------------|--------------|---------------|------------------|
| H                | x   | x               | x               | x               | x               | High-Z       | High-Z        | Standby          |
| x                | L   | x               | x               | x               | x               | High-Z       | High-Z        | Standby          |
| x                | x   | x               | x               | H               | H               | High-Z       | High-Z        | Standby          |
| L                | H   | H               | L               | L               | L               | Dout         | Dout          | Read             |
| L                | H   | H               | L               | H               | L               | Dout         | High-Z        | Lower byte read  |
| L                | H   | H               | L               | L               | H               | High-Z       | Dout          | Upper byte read  |
| L                | H   | L               | x               | L               | L               | Din          | Din           | Write            |
| L                | H   | L               | x               | H               | L               | Din          | High-Z        | Lower byte write |
| L                | H   | L               | x               | L               | H               | High-Z       | Din           | Upper byte write |
| L                | H   | H               | H               | x               | x               | High-Z       | High-Z        | Output disable   |

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , x:  $V_{IH}$  or  $V_{IL}$

## Absolute Maximum Ratings

| Parameter                                        | Symbol   | Value                                              | Unit |
|--------------------------------------------------|----------|----------------------------------------------------|------|
| Power supply voltage relative to $V_{SS}$        | $V_{CC}$ | -0.5 to + 4.6                                      | V    |
| Terminal voltage on any pin relative to $V_{SS}$ | $V_T$    | -0.5 <sup>*1</sup> to $V_{CC} + 0.3$ <sup>*2</sup> | V    |
| Power dissipation                                | $P_T$    | 1.0                                                | W    |
| Storage temperature range                        | Tstg     | -55 to +125                                        | °C   |
| Storage temperature range under bias             | Tbias    | -40 to +85                                         | °C   |

Notes: 1.  $V_T$  min: -3.0 V for pulse half-width  $\leq 30$  ns.

2. Maximum voltage is +4.6 V.

## DC Operating Conditions

| Parameter                 | Symbol                             | Min  | Typ     | Max            | Unit | Note |
|---------------------------|------------------------------------|------|---------|----------------|------|------|
| Supply voltage            | $V_{CC}$                           | 2.2  | 2.5/3.0 | 3.6            | V    |      |
|                           | $V_{SS}$                           | 0    | 0       | 0              | V    |      |
| Input high voltage        | $V_{CC} = 2.2$ V to 2.7 V $V_{IH}$ | 2.0  | —       | $V_{CC} + 0.3$ | V    |      |
|                           | $V_{CC} = 2.7$ V to 3.6 V $V_{IH}$ | 2.2  | —       | $V_{CC} + 0.3$ | V    |      |
| Input low voltage         | $V_{CC} = 2.2$ V to 2.7 V $V_{IL}$ | -0.2 | —       | 0.4            | V    | 1    |
|                           | $V_{CC} = 2.7$ V to 3.6 V $V_{IL}$ | -0.3 | —       | 0.6            | V    | 1    |
| Ambient temperature range | Ta                                 | -40  | —       | 85             | °C   |      |

Note: 1.  $V_{IL}$  min: -3.0 V for pulse half-width  $\leq 30$  ns.

## DC Characteristics

| Parameter                 | Symbol                                              | Min            | Typ* <sup>1</sup> | Max | Unit          | Test conditions                                                                                                                                                                                                                                                                                                |
|---------------------------|-----------------------------------------------------|----------------|-------------------|-----|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Input leakage current     | $ I_{LI} $                                          | —              | —                 | 1   | $\mu\text{A}$ | $V_{in} = V_{SS}$ to $V_{CC}$                                                                                                                                                                                                                                                                                  |
| Output leakage current    | $ I_{LO} $                                          | —              | —                 | 1   | $\mu\text{A}$ | $\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or<br>$\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or<br>$\overline{LB} = \overline{UB} = V_{IH}$ ,<br>$V_{I/O} = V_{SS}$ to $V_{CC}$                                                                                                                      |
| Operating current         | $I_{CC}$                                            | —              | 5                 | 20  | $\text{mA}$   | $\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ ,<br>Others = $V_{IH}/V_{IL}$ , $I_{I/O} = 0 \text{ mA}$                                                                                                                                                                                                            |
| Average operating current | $I_{CC1}$                                           | —              | 7                 | 25  | $\text{mA}$   | Min. cycle, duty = 100%,<br>$I_{I/O} = 0 \text{ mA}$ , $\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ ,<br>Others = $V_{IH}/V_{IL}$                                                                                                                                                                                |
|                           | $I_{CC2}$                                           | —              | 2                 | 5   | $\text{mA}$   | Cycle time = 1 $\mu\text{s}$ , duty = 100%,<br>$I_{I/O} = 0 \text{ mA}$ , $\overline{CS1} \leq 0.2 \text{ V}$ ,<br>$CS2 \geq V_{CC} - 0.2 \text{ V}$ ,<br>$V_{IH} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IL} \leq 0.2 \text{ V}$                                                                                   |
| Standby current           | $I_{SB}$                                            | —              | 0.1               | 0.3 | $\text{mA}$   | $CS2 = V_{IL}$                                                                                                                                                                                                                                                                                                 |
| Standby current           | $I_{SB1}^{*2}$                                      | —              | 0.8               | 20  | $\mu\text{A}$ | 0 V $\leq V_{in}$<br>(1) 0 V $\leq CS2 \leq 0.2 \text{ V}$ or<br>(2) $\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$ ,<br>$CS2 \geq V_{CC} - 0.2 \text{ V}$ or<br>(3) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2 \text{ V}$ ,<br>$CS2 \geq V_{CC} - 0.2 \text{ V}$ ,<br>$\overline{CS1} \leq 0.2 \text{ V}$ |
| Output high voltage       | $V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$ $V_{OH}$ | 2.0            | —                 | —   | $\text{V}$    | $I_{OH} = -0.5 \text{ mA}$                                                                                                                                                                                                                                                                                     |
|                           | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ $V_{OH}$ | 2.4            | —                 | —   | $\text{V}$    | $I_{OH} = -1 \text{ mA}$                                                                                                                                                                                                                                                                                       |
|                           | $V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$ $V_{OH}$ | $V_{CC} - 0.2$ | —                 | —   | $\text{V}$    | $I_{OH} = -100 \mu\text{A}$                                                                                                                                                                                                                                                                                    |
| Output low voltage        | $V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$ $V_{OL}$ | —              | —                 | 0.4 | $\text{V}$    | $I_{OL} = 0.5 \text{ mA}$                                                                                                                                                                                                                                                                                      |
|                           | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ $V_{OL}$ | —              | —                 | 0.4 | $\text{V}$    | $I_{OL} = 2 \text{ mA}$                                                                                                                                                                                                                                                                                        |
|                           | $V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$ $V_{OL}$ | —              | —                 | 0.2 | $\text{V}$    | $I_{OL} = 100 \mu\text{A}$                                                                                                                                                                                                                                                                                     |

Notes: 1. Typical values are at  $V_{CC} = 2.5 \text{ V}/3.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.

2. This characteristic is guaranteed only for L-version.

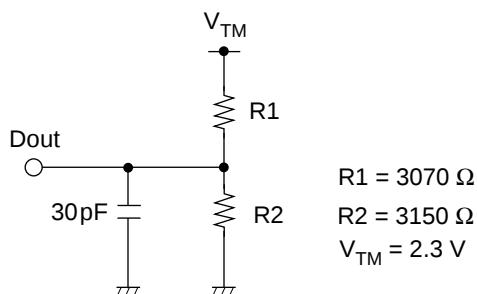
## Capacitance ( $T_a = +25^\circ\text{C}$ , $f = 1.0 \text{ MHz}$ )

| Parameter                | Symbol    | Min | Typ | Max | Unit        | Test conditions         | Note |
|--------------------------|-----------|-----|-----|-----|-------------|-------------------------|------|
| Input capacitance        | $C_{in}$  | —   | —   | 8   | $\text{pF}$ | $V_{in} = 0 \text{ V}$  | 1    |
| Input/output capacitance | $C_{I/O}$ | —   | —   | 10  | $\text{pF}$ | $V_{I/O} = 0 \text{ V}$ | 1    |

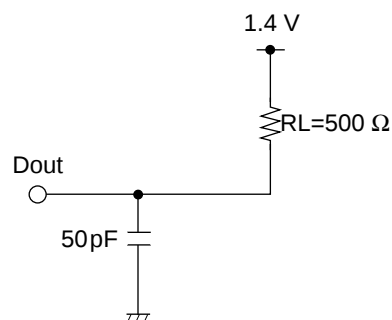
Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics** ( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.2$  V to  $3.6$  V, unless otherwise noted.)**Test Conditions**

- Input pulse levels:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.2$  V ( $V_{CC} = 2.2$  V to  $2.7$  V)  
:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.4$  V ( $V_{CC} = 2.7$  V to  $3.6$  V)
- Input rise and fall time: 5 ns
- Input/output timing reference levels:  $1.1$  V ( $V_{CC} = 2.2$  V to  $2.7$  V)  
:  $1.4$  V ( $V_{CC} = 2.7$  V to  $3.6$  V)
- Output load: See figures (Including scope and jig)



Output load (A)  
( $V_{CC} = 2.2$  V to  $2.7$  V)



Output load (B)  
( $V_{CC} = 2.7$  V to  $3.6$  V)

# HM62V16256CI Series

## Read Cycle

|                                                                   |                   | HM62V16256CI |     |      |         |
|-------------------------------------------------------------------|-------------------|--------------|-----|------|---------|
|                                                                   |                   | -7           |     |      |         |
| Parameter                                                         | Symbol            | Min          | Max | Unit | Notes   |
| Read cycle time                                                   | t <sub>RC</sub>   | 70           | —   | ns   |         |
| Address access time                                               | t <sub>AA</sub>   | —            | 70  | ns   |         |
| Chip select access time                                           | t <sub>ACS1</sub> | —            | 70  | ns   |         |
|                                                                   | t <sub>ACS2</sub> | —            | 70  | ns   |         |
| Output enable to output valid                                     | t <sub>OE</sub>   | —            | 40  | ns   |         |
| Output hold from address change                                   | t <sub>OH</sub>   | 10           | —   | ns   |         |
| $\overline{\text{LB}}$ , $\overline{\text{UB}}$ access time       | t <sub>BA</sub>   | —            | 70  | ns   |         |
| Chip select to output in low-Z                                    | t <sub>CLZ1</sub> | 10           | —   | ns   | 2, 3    |
|                                                                   | t <sub>CLZ2</sub> | 10           | —   | ns   | 2, 3    |
| $\overline{\text{LB}}$ , $\overline{\text{UB}}$ enable to low-z   | t <sub>BLZ</sub>  | 5            | —   | ns   | 2, 3    |
| Output enable to output in low-Z                                  | t <sub>OLZ</sub>  | 5            | —   | ns   | 2, 3    |
| Chip deselect to output in high-Z                                 | t <sub>CHZ1</sub> | 0            | 25  | ns   | 1, 2, 3 |
|                                                                   | t <sub>CHZ2</sub> | 0            | 25  | ns   | 1, 2, 3 |
| $\overline{\text{LB}}$ , $\overline{\text{UB}}$ disable to high-Z | t <sub>BHZ</sub>  | 0            | 25  | ns   | 1, 2, 3 |
| Output disable to output in high-Z                                | t <sub>OHZ</sub>  | 0            | 25  | ns   | 1, 2, 3 |

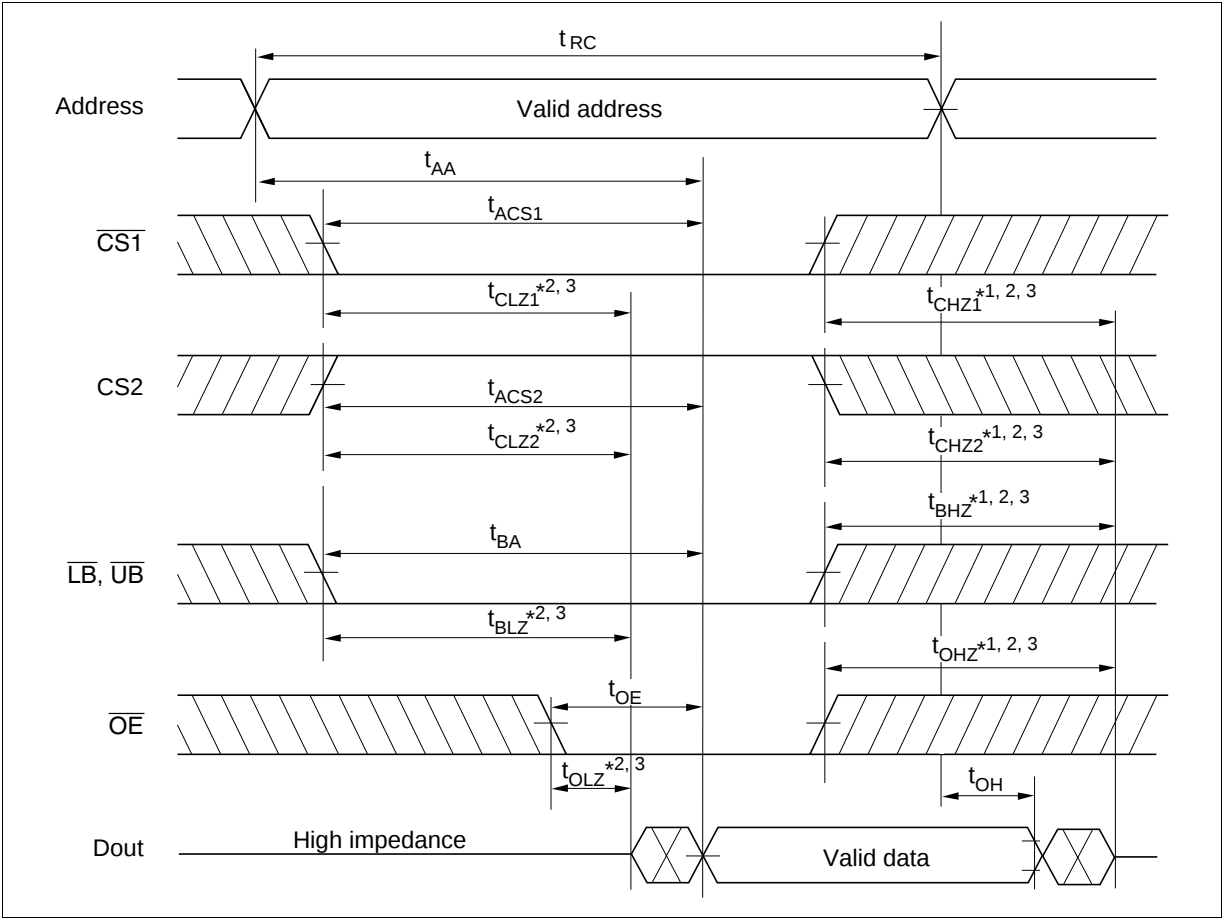
## Write Cycle

|                                                         |                  | HM62V16256CI |     |      |       |
|---------------------------------------------------------|------------------|--------------|-----|------|-------|
|                                                         |                  | -7           |     |      |       |
| Parameter                                               | Symbol           | Min          | Max | Unit | Notes |
| Write cycle time                                        | t <sub>WC</sub>  | 70           | —   | ns   |       |
| Address valid to end of write                           | t <sub>AW</sub>  | 60           | —   | ns   |       |
| Chip selection to end of write                          | t <sub>CW</sub>  | 60           | —   | ns   | 5     |
| Write pulse width                                       | t <sub>WP</sub>  | 50           | —   | ns   | 4     |
| $\overline{LB}$ , $\overline{UB}$ valid to end of write | t <sub>BW</sub>  | 55           | —   | ns   |       |
| Address setup time                                      | t <sub>AS</sub>  | 0            | —   | ns   | 6     |
| Write recovery time                                     | t <sub>WR</sub>  | 0            | —   | ns   | 7     |
| Data to write time overlap                              | t <sub>DW</sub>  | 30           | —   | ns   |       |
| Data hold from write time                               | t <sub>DH</sub>  | 0            | —   | ns   |       |
| Output active from end of write                         | t <sub>OW</sub>  | 5            | —   | ns   | 2     |
| Output disable to output in High-Z                      | t <sub>OHZ</sub> | 0            | 25  | ns   | 1, 2  |
| Write to output in high-Z                               | t <sub>WHZ</sub> | 0            | 25  | ns   | 1, 2  |

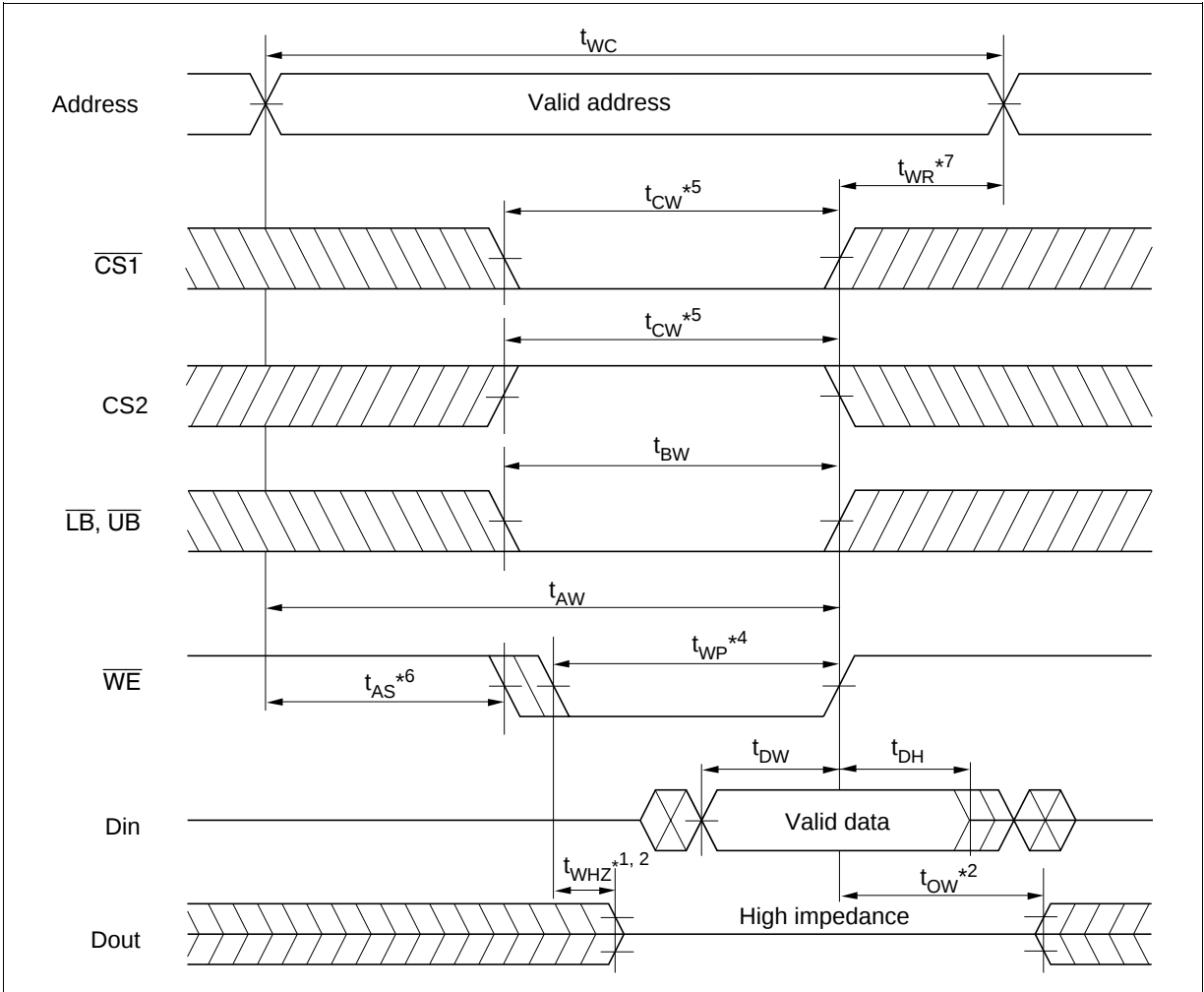
- Notes: 1.  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  and  $t_{BHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
4. A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2, a low  $\overline{WE}$  and a low  $\overline{LB}$  or a low  $\overline{UB}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high,  $\overline{WE}$  going low and  $\overline{LB}$  going low or  $\overline{UB}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low,  $\overline{WE}$  going high and  $\overline{LB}$  going high or  $\overline{UB}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
5.  $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or CS2 going high to the end of write.
6.  $t_{AS}$  is measured from the address valid to the beginning of write.
7.  $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going low to the end of write cycle.

Timing Waveform

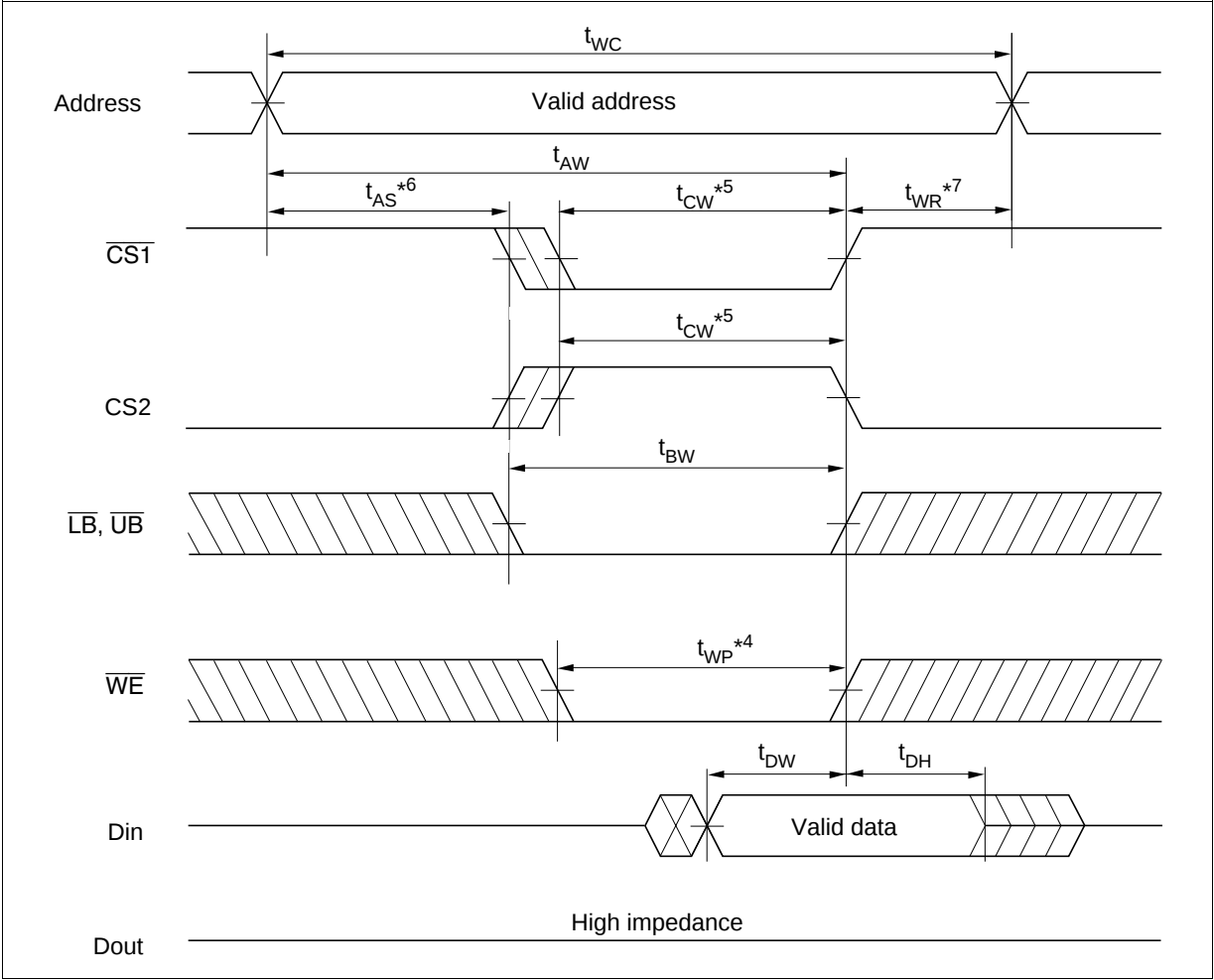
Read Cycle



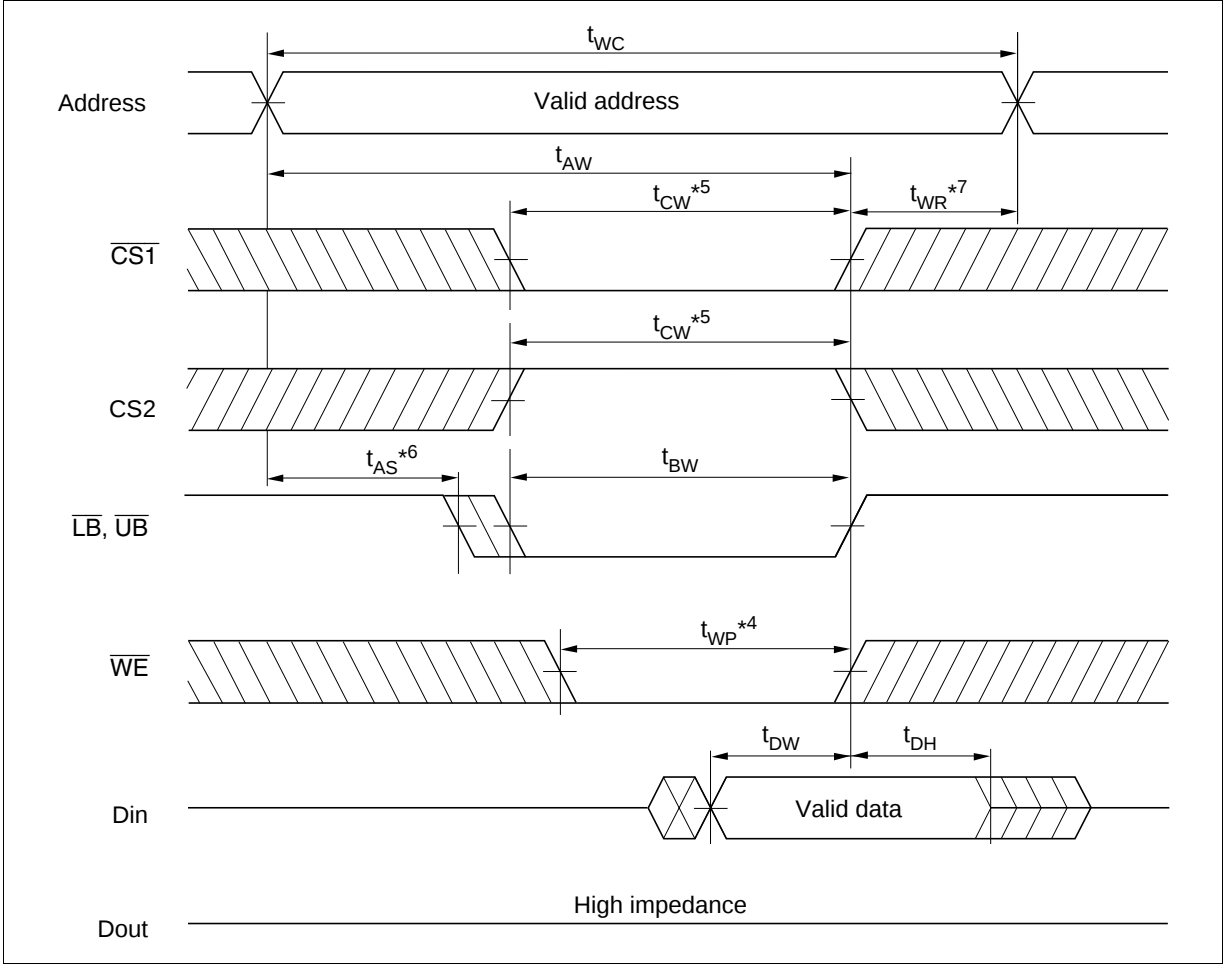
Write Cycle (1) ( $\overline{\text{WE}}$  Clock)



Write Cycle (2) ( $\overline{\text{CS}}$  Clock,  $\overline{\text{OE}} = V_{\text{IH}}$ )



Write Cycle (3) ( $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$  Clock,  $\overline{\text{OE}} = V_{\text{IH}}$ )

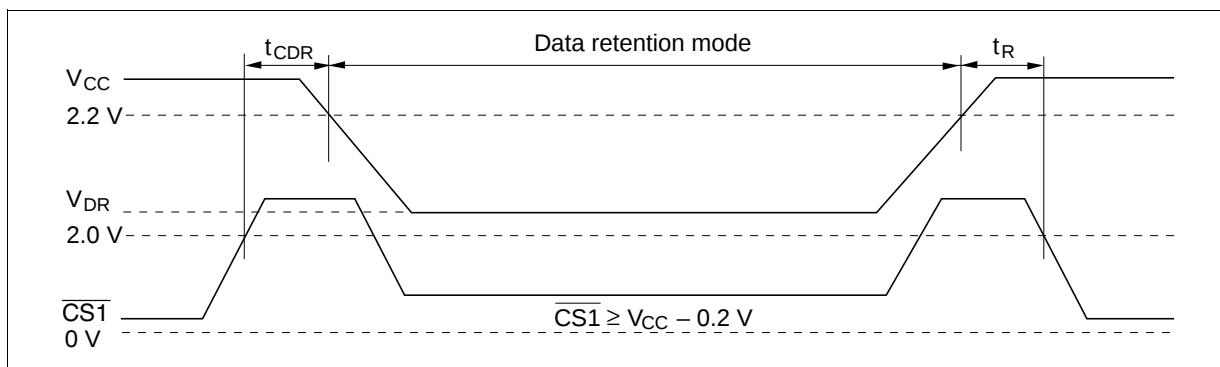


## Low $V_{CC}$ Data Retention Characteristics ( $T_a = -40$ to $+85^{\circ}\text{C}$ )

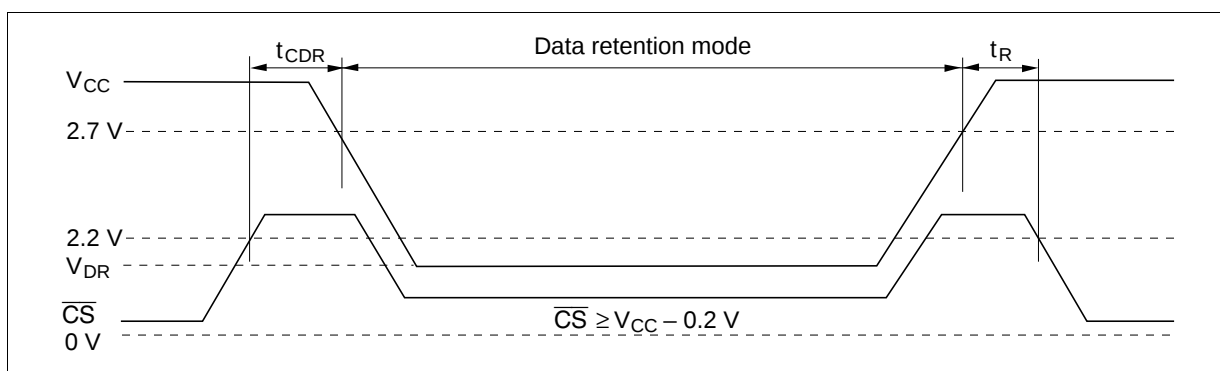
| Parameter                            | Symbol          | Min           | Typ <sup>*3</sup> | Max | Unit          | Test conditions <sup>*2</sup>                                                                                                                                                                                                                                            |
|--------------------------------------|-----------------|---------------|-------------------|-----|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{CC}$ for data retention          | $V_{DR}$        | 2.0           | —                 | 3.6 | V             | $V_{in} \geq 0V$<br>(1) $0V \leq CS2 \leq 0.2V$ or<br>(2) $CS2 \geq V_{CC} - 0.2V$ ,<br>$\overline{CS1} \geq V_{CC} - 0.2V$ or<br>(3) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$ ,<br>$CS2 \geq V_{CC} - 0.2V$ ,<br>$\overline{CS1} \leq 0.2V$                   |
| Data retention current               | $I_{CCDR}^{*1}$ | —             | 0.8               | 20  | $\mu\text{A}$ | $V_{CC} = 3.0V$ , $V_{in} \geq 0V$<br>(1) $0V \leq CS2 \leq 0.2V$ or<br>(2) $CS2 \geq V_{CC} - 0.2V$ ,<br>$\overline{CS1} \geq V_{CC} - 0.2V$ or<br>(3) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$ ,<br>$CS2 \geq V_{CC} - 0.2V$ ,<br>$\overline{CS1} \leq 0.2V$ |
| Chip deselect to data retention time | $t_{CDR}$       | 0             | —                 | —   | ns            | See retention waveform                                                                                                                                                                                                                                                   |
| Operation recovery time              | $t_R$           | $t_{RC}^{*4}$ | —                 | —   | ns            |                                                                                                                                                                                                                                                                          |

- Notes: 1. This characteristic is guaranteed only for L-version, 10  $\mu\text{A}$  max. at  $T_a = -40$  to  $+40^{\circ}\text{C}$ .
2. CS2 controls address buffer,  $\overline{WE}$  buffer,  $\overline{CS1}$  buffer,  $\overline{OE}$  buffer,  $\overline{LB}$ ,  $\overline{UB}$  buffer and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{CS1}$ ,  $\overline{LB}$ ,  $\overline{UB}$ , I/O) can be in the high impedance state. If  $\overline{CS1}$  controls data retention mode, CS2 must be  $CS2 \geq V_{CC} - 0.2V$  or  $0V \leq CS2 \leq 0.2V$ . The other input levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{LB}$ ,  $\overline{UB}$ , I/O) can be in the high impedance state.
3. Typical values are at  $V_{CC} = 3.0V$ ,  $T_a = +25^{\circ}\text{C}$  and not guaranteed.
4.  $t_{RC}$  = read cycle time.

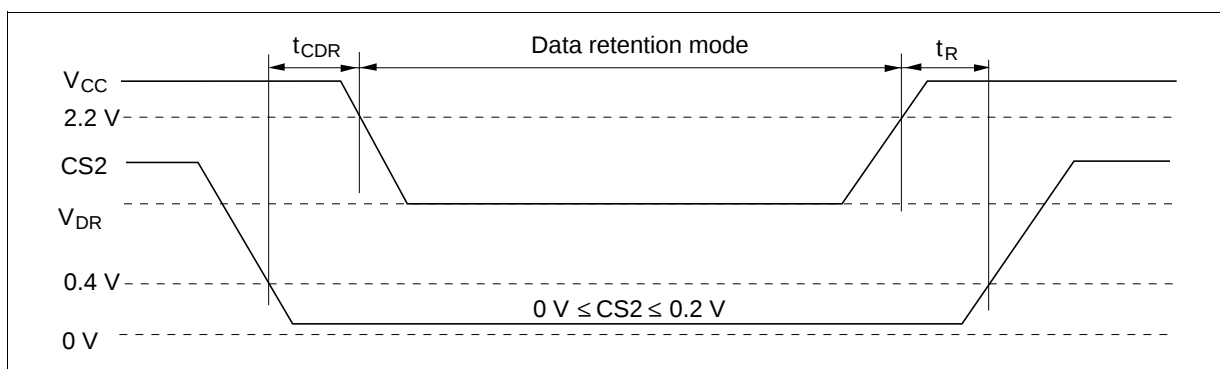
**Low  $V_{CC}$  Data Retention Timing Waveform (1) ( $\overline{CS1}$  Controlled) ( $V_{CC} = 2.2\text{ V}$  to  $2.7\text{ V}$ )**



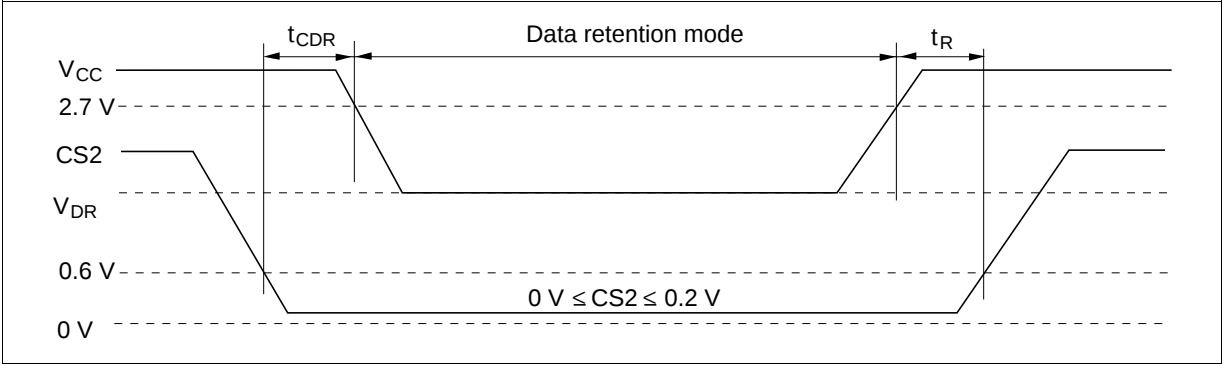
**Low  $V_{CC}$  Data Retention Timing Waveform (2) ( $\overline{CS1}$  Controlled) ( $V_{CC} = 2.7\text{ V}$  to  $3.6\text{ V}$ )**



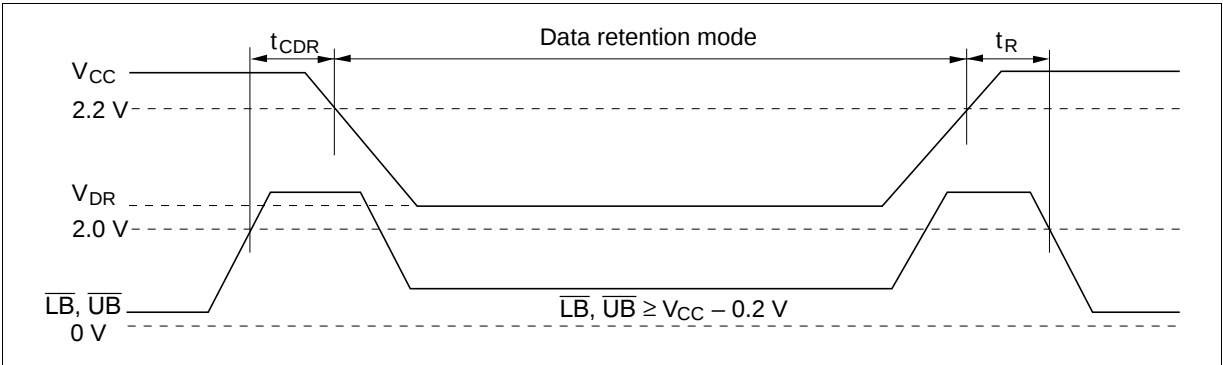
**Low  $V_{CC}$  Data Retention Timing Waveform (3) ( $CS2$  Controlled) ( $V_{CC} = 2.2\text{ V}$  to  $2.7\text{ V}$ )**



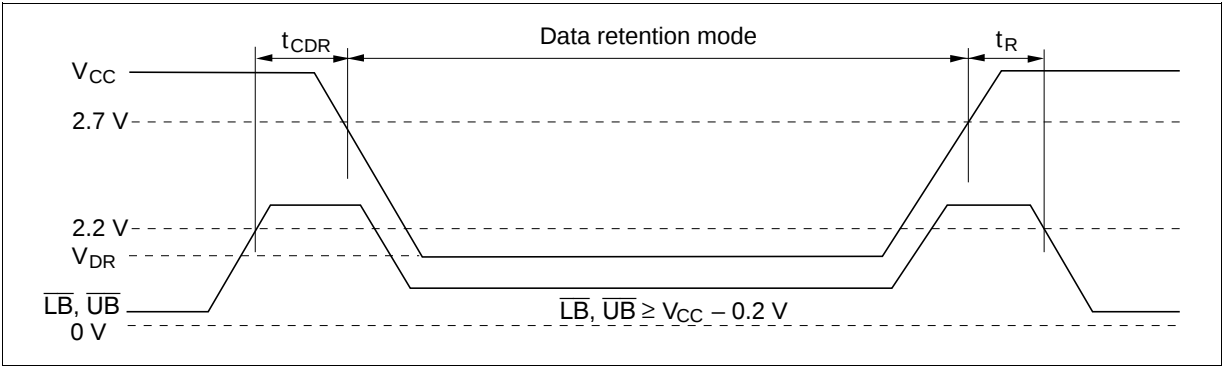
Low  $V_{CC}$  Data Retention Timing Waveform (4) (CS2 Controlled) ( $V_{CC} = 2.7\text{ V}$  to  $3.6\text{ V}$ )



Low  $V_{CC}$  Data Retention Timing Waveform (5) ( $\overline{LB}$ ,  $\overline{UB}$  Controlled) ( $V_{CC} = 2.2\text{ V}$  to  $2.7\text{ V}$ )



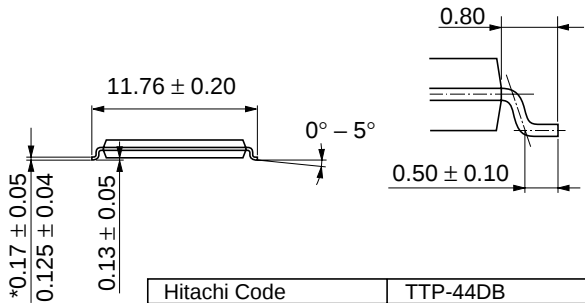
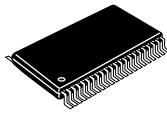
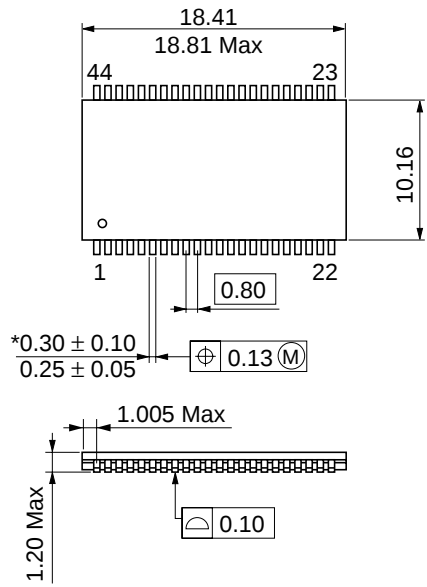
Low  $V_{CC}$  Data Retention Timing Waveform (6) ( $\overline{LB}$ ,  $\overline{UB}$  Controlled) ( $V_{CC} = 2.7\text{ V}$  to  $3.6\text{ V}$ )



Package Dimensions

HM62V16256CLTTI Series (TTP-44DB)

As of January, 2001  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

|                        |          |
|------------------------|----------|
| Hitachi Code           | TTP-44DB |
| JEDEC                  | —        |
| EIAJ                   | —        |
| Mass (reference value) | 0.43 g   |

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