

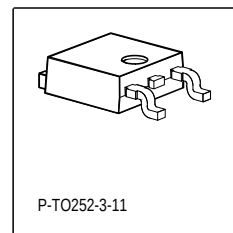
Smart Lowside Power Switch

Features

- Logic Level Input
- Input Protection (ESD)
- Thermal shutdown with auto restart
- Overload protection
- Short circuit protection
- Overvoltage protection
- Current limitation
- Analog driving possible

Product Summary

Drain source voltage	V_{DS}	42	V
On-state resistance	$R_{DS(on)}$	100	m Ω
Nominal load current	$I_{D(Nom)}$	2.4	A
Clamping energy	E_{AS}	2	J

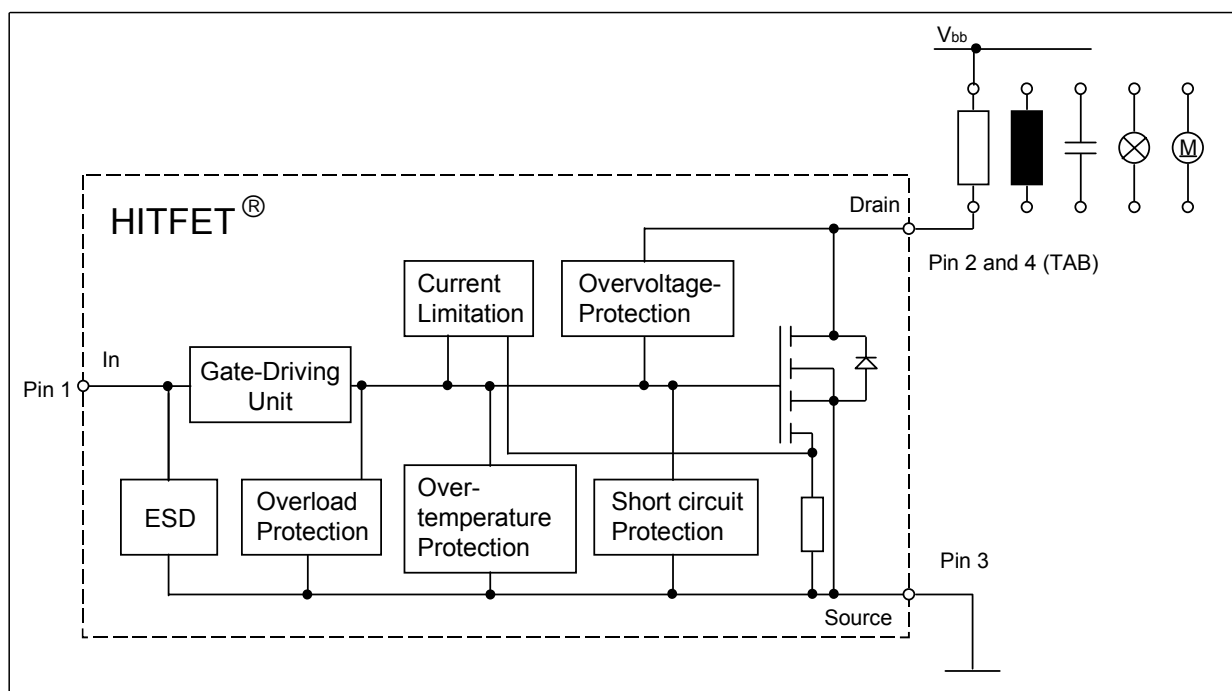


Application

- All kinds of resistive, inductive and capacitive loads in switching or linear applications
- μ C compatible power switch for 12 V DC applications
- Replaces electromechanical relays and discrete circuits

General Description

N channel vertical power FET in Smart SIPMOS® technology. Fully protected by embedded protection functions.



Complete product spectrum and additional information <http://www.infineon.com/hitfet>

Maximum Ratings at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	42	V
Supply voltage for full short circuit protection	$V_{bb(SC)}$	42	
Continuous input voltage ¹⁾	V_{IN}	-0.2 ²⁾ ... +10	
Continuous input current ²⁾ -0.2V $\leq V_{IN} \leq$ 10V $V_{IN} < -0.2\text{V}$ or $V_{IN} > 10\text{V}$	I_{IN}	self limited $ I_{IN} \leq 2$	mA
Operating temperature	T_j	-40 ... +150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 ... +150	
Power dissipation ⁵⁾ $T_C = 85^\circ\text{C}$ 6cm ² cooling area , $T_A = 85^\circ\text{C}$	P_{tot}	21 1.1	W
Unclamped single pulse inductive energy ²⁾	E_{AS}	2	J
Load dump protection $V_{LoadDump}^{2)3)} = V_A + V_S$ $V_{IN} = 0$ and 10 V, $t_d = 400$ ms, $R_I = 2\ \Omega$, $R_L = 6\ \Omega$, $V_A = 13.5$ V	V_{LD}	58	V
Electrostatic discharge voltage²⁾ (Human Body Model) according to Jedec norm EIA/JESD22-A114-B, Section 4	V_{ESD}	2	kV
Jedec humidity category, J-STD-20-B		MSL1	
IEC climatic category; DIN EN 60068-1		40/150/56	

Thermal resistance

junction - case:	R_{thJC}	3	K/W
SMD: junction - ambient @ min. footprint @ 6 cm ² cooling area ⁴⁾	R_{thJA}	115 55	

¹⁾For input voltages beyond these limits I_{IN} has to be limited.

²⁾not subject to production test, specified by design

³⁾ $V_{Loaddump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

⁴⁾ Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB mounted vertical without blown air.

⁵⁾not subject to production test, calculated by R_{thJA} and $R_{ds(on)}$

Electrical Characteristics

Parameter at $T_j = 25^{\circ}\text{C}$, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Drain source clamp voltage $T_j = -40 \dots +150$, $I_D = 10 \text{ mA}$	$V_{\text{DS(AZ)}}$	42	-	55	V
Off-state drain current $T_j = -40\dots+85^{\circ}\text{C}$, $V_{\text{DS}} = 32 \text{ V}$, $V_{\text{IN}} = 0 \text{ V}$ $T_j = 150^{\circ}\text{C}$	I_{DSS}	- -	1.5 4	8 12	μA
Input threshold voltage $I_D = 0.6 \text{ mA}$, $T_j = 25^{\circ}\text{C}$ $I_D = 0.6 \text{ mA}$, $T_j = 150^{\circ}\text{C}$	$V_{\text{IN(th)}}$	1.3 0.8	1.7 -	2.2 -	V
On state input current	$I_{\text{IN(on)}}$	-	10	30	μA
On-state resistance $V_{\text{IN}} = 5 \text{ V}$, $I_D = 2.2 \text{ A}$, $T_j = 25^{\circ}\text{C}$ $V_{\text{IN}} = 5 \text{ V}$, $I_D = 2.2 \text{ A}$, $T_j = 150^{\circ}\text{C}$	$R_{\text{DS(on)}}$	- -	90 160	120 240	$\text{m}\Omega$
On-state resistance $V_{\text{IN}} = 10 \text{ V}$, $I_D = 2.2 \text{ A}$, $T_j = 25^{\circ}\text{C}$ $V_{\text{IN}} = 10 \text{ V}$, $I_D = 2.2 \text{ A}$, $T_j = 150^{\circ}\text{C}$	$R_{\text{DS(on)}}$	- -	70 130	100 200	
Nominal load current ⁵⁾ $T_j < 150^{\circ}\text{C}$, $V_{\text{IN}} = 10 \text{ V}$, $T_{\text{A}} = 85^{\circ}\text{C}$, SMD ¹⁾	$I_{\text{D(Nom)}}$	2.4	3.2	-	
Nominal load current ⁵⁾ $V_{\text{IN}} = 10 \text{ V}$, $V_{\text{DS}} = 0.5 \text{ V}$, $T_{\text{C}} = 85^{\circ}\text{C}$, $T_j < 150^{\circ}\text{C}$	$I_{\text{D(ISO)}}$	3.5	5	-	
Current limit (active if $V_{\text{DS}} > 2.5 \text{ V}$) ²⁾ $V_{\text{IN}} = 10 \text{ V}$, $V_{\text{DS}} = 12 \text{ V}$, $t_{\text{m}} = 200 \mu\text{s}$	$I_{\text{D(lim)}}$	10	15	20	

¹⁾@ 6 cm² cooling area

²⁾Device switched on into existing short circuit (see diagram Determination of $I_{D(lim)}$). If the device is in on condition and a short circuit occurs, these values might be exceeded for max. 50 μs .

⁵⁾not subject to production test, calculated by R_{thJA} and $R_{ds(on)}$

Electrical Characteristics

Parameter at $T_j = 25^\circ\text{C}$, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	

Dynamic Characteristics

Turn-on time V_{IN} to 90% I_D : $R_L = 4.7\ \Omega$, $V_{IN} = 0$ to 10 V, $V_{bb} = 12$ V	t_{on}	-	40	100	μs
Turn-off time V_{IN} to 10% I_D : $R_L = 4.7\ \Omega$, $V_{IN} = 10$ to 0 V, $V_{bb} = 12$ V	t_{off}	-	70	100	μs
Slew rate on 70 to 50% V_{bb} : $R_L = 4.7\ \Omega$, $V_{IN} = 0$ to 10 V, $V_{bb} = 12$ V	$-dV_{DS}/dt_{on}$	-	0.4	1.5	V/ μs
Slew rate off 50 to 70% V_{bb} : $R_L = 4.7\ \Omega$, $V_{IN} = 10$ to 0 V, $V_{bb} = 12$ V	dV_{DS}/dt_{off}	-	0.6	1.5	V/ μs

Protection Functions¹⁾

Thermal overload trip temperature	T_{jt}	150	175	-	$^\circ\text{C}$
Thermal hysteresis ²⁾	ΔT_{jt}	-	10	-	K
Input current protection mode $T_j = 150\ ^\circ\text{C}$	$I_{IN(Prot)}$	-	100	300	μA
Unclamped single pulse inductive energy ²⁾ $I_D = 2.2$ A, $T_j = 25\ ^\circ\text{C}$, $V_{bb} = 12$ V	E_{AS}	2	-	-	J

Inverse Diode

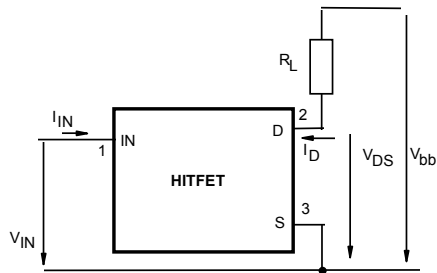
Inverse diode forward voltage $I_F = 10.9$ A, $t_m = 250\ \mu\text{s}$, $V_{IN} = 0$ V, $t_P = 300\ \mu\text{s}$	V_{SD}	-	1.0	1.5	V
---	----------	---	-----	-----	---

¹⁾ Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

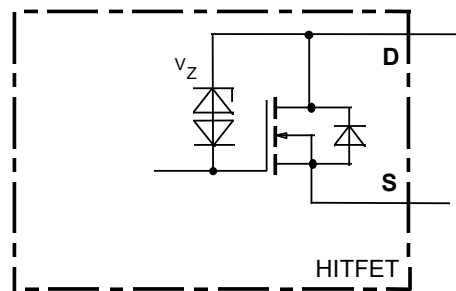
²⁾ not subject to production test, specified by design

Block diagram

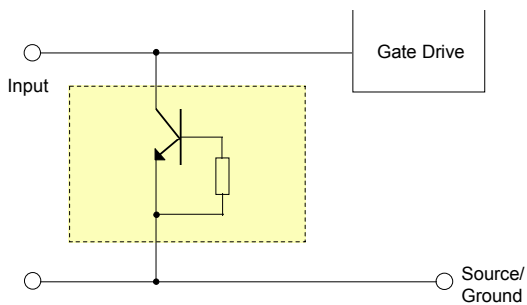
Terms



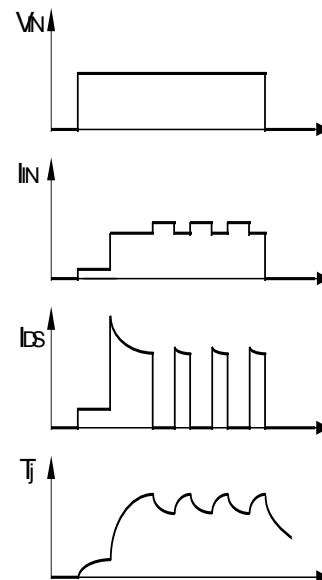
Inductive and overvoltage output clamp



Input circuit (ESD protection)



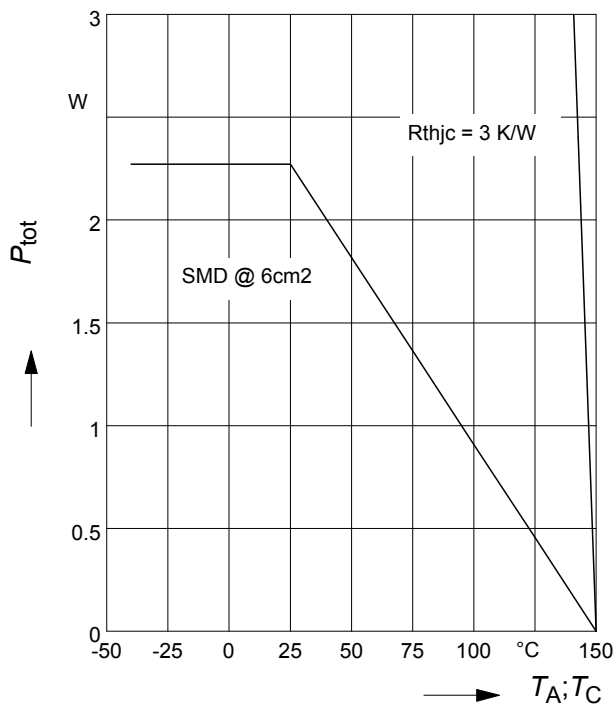
Short circuit behaviour



1 Maximum allowable power dissipation

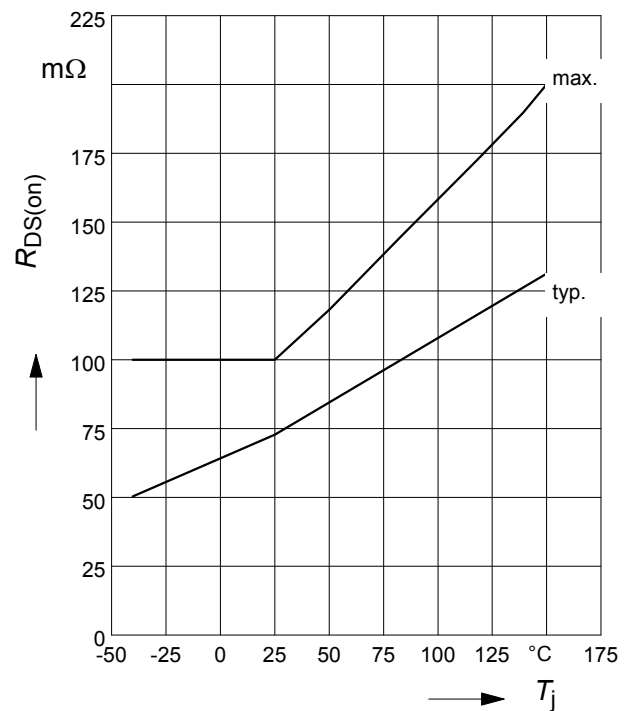
$$P_{\text{tot}} = f(T_C) \text{ resp.}$$

$$P_{\text{tot}} = f(T_A) @ R_{\text{thJA}} = 55 \text{ K/W}$$



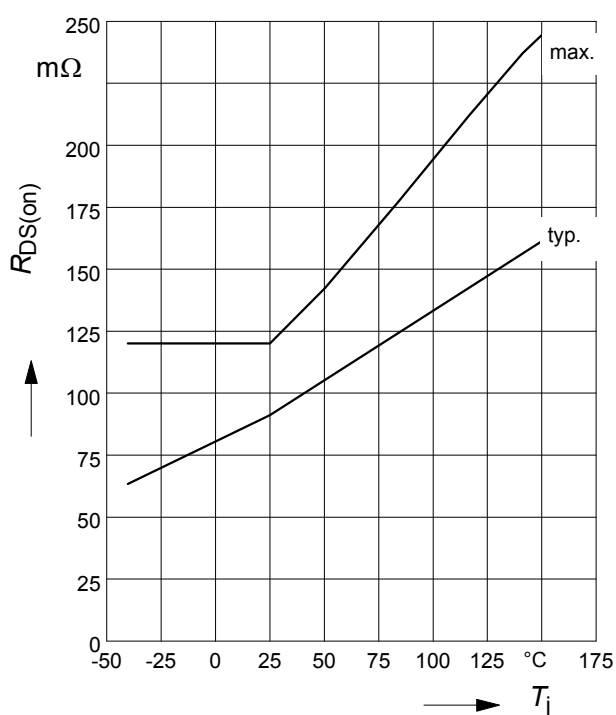
2 On-state resistance

$$R_{\text{ON}} = f(T_j); I_D = 2.2 \text{ A}; V_{\text{IN}} = 10 \text{ V}$$



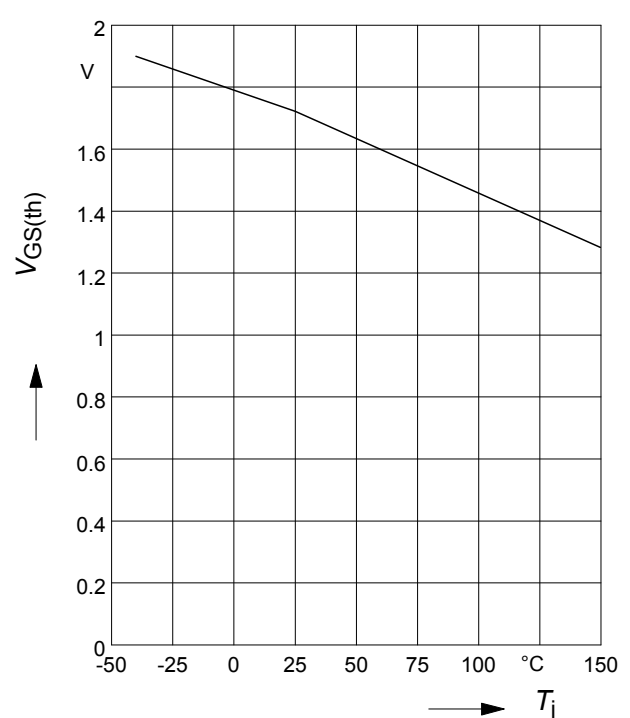
3 On-state resistance

$$R_{\text{ON}} = f(T_j); I_D = 2.2 \text{ A}; V_{\text{IN}} = 5 \text{ V}$$

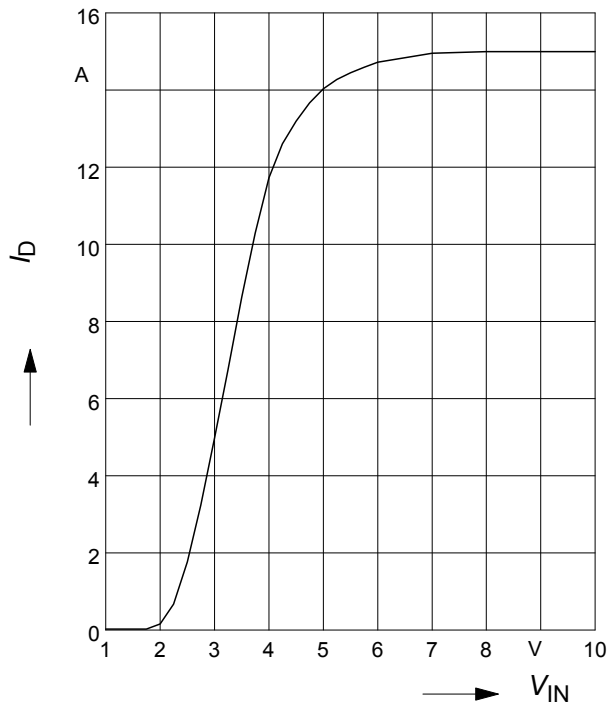


4 Typ. input threshold voltage

$$V_{\text{IN(th)}} = f(T_j); I_D = 0.3 \text{ mA}; V_{\text{DS}} = 12 \text{ V}$$

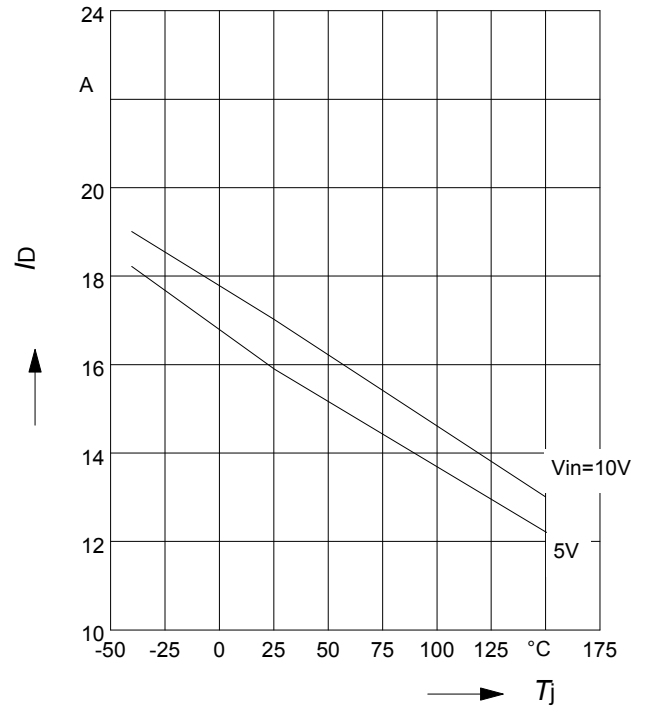


5 Typ. transfer characteristics

 $I_D = f(V_{IN}); V_{DS} = 12V; T_{Jstart} = 25^\circ C$


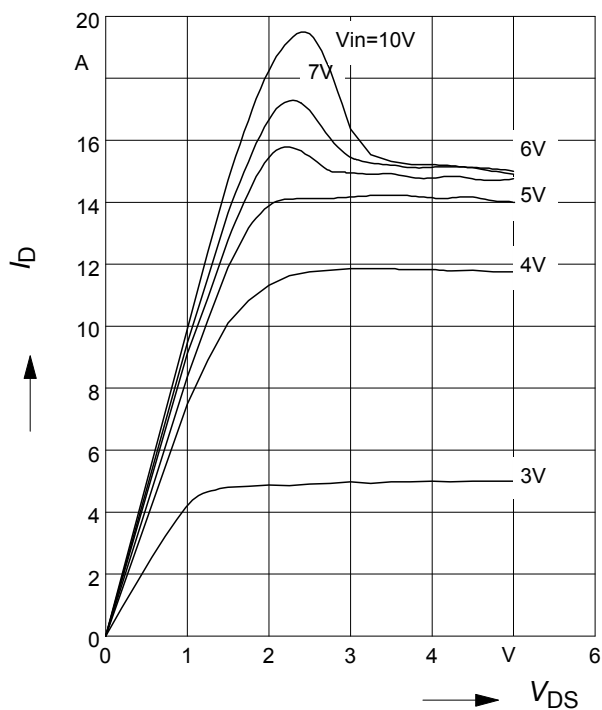
6 Typ. short circuit current

 $I_{D(lim)} = f(T_J); V_{DS} = 12V$

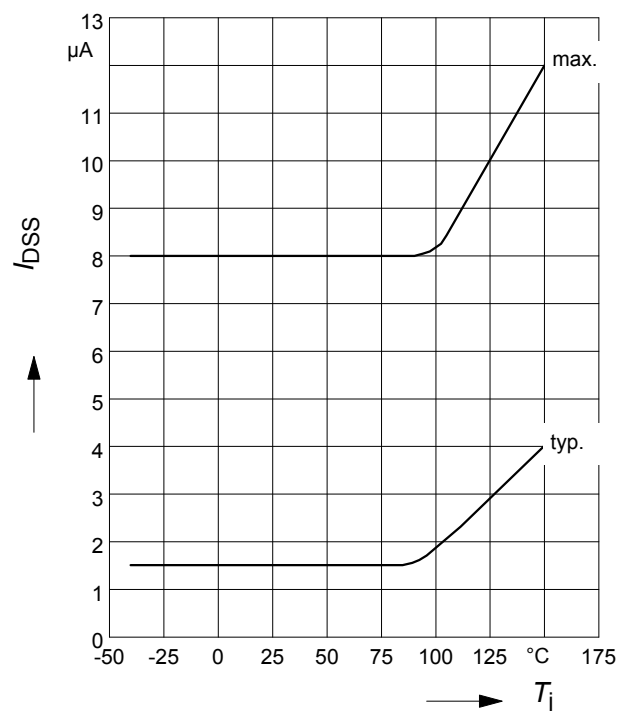
Parameter: V_{IN}


7 Typ. output characteristics

 $I_D = f(V_{DS}); T_{Jstart} = 25^\circ C$

Parameter: V_{IN}


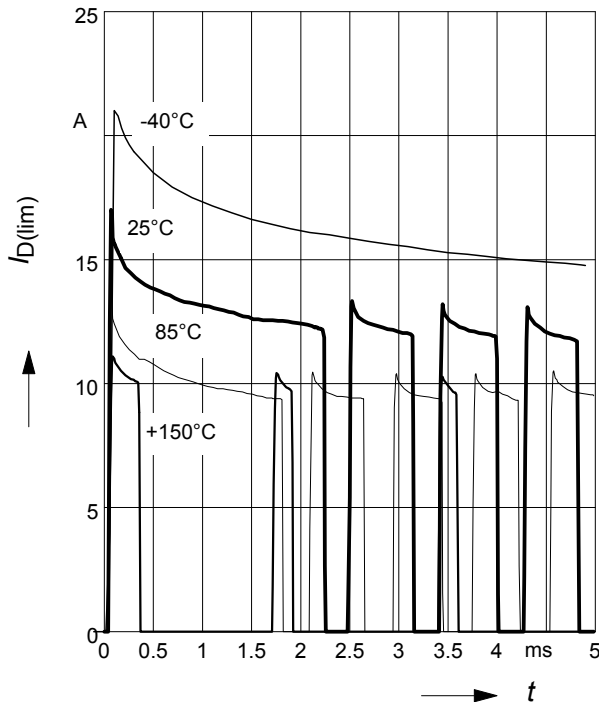
8 Off-state drain current

 $I_{DSS} = f(T_J)$


9 Typ. overload current

$I_{D(lim)} = f(t)$, $V_{bb}=12\text{ V}$, no heatsink

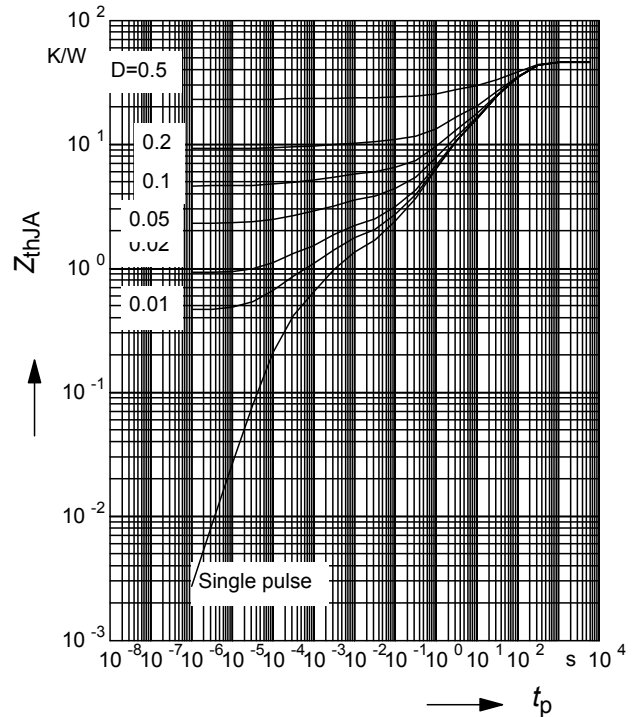
Parameter: T_{jstart}



10 Typ. transient thermal impedance

$Z_{thJA}=f(t_p)$ @ 6 cm^2 cooling area

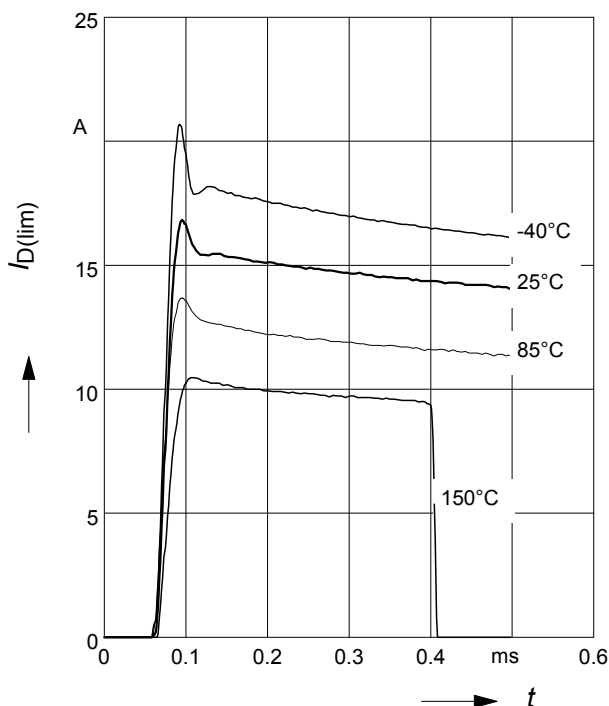
Parameter: $D=t_p/T$

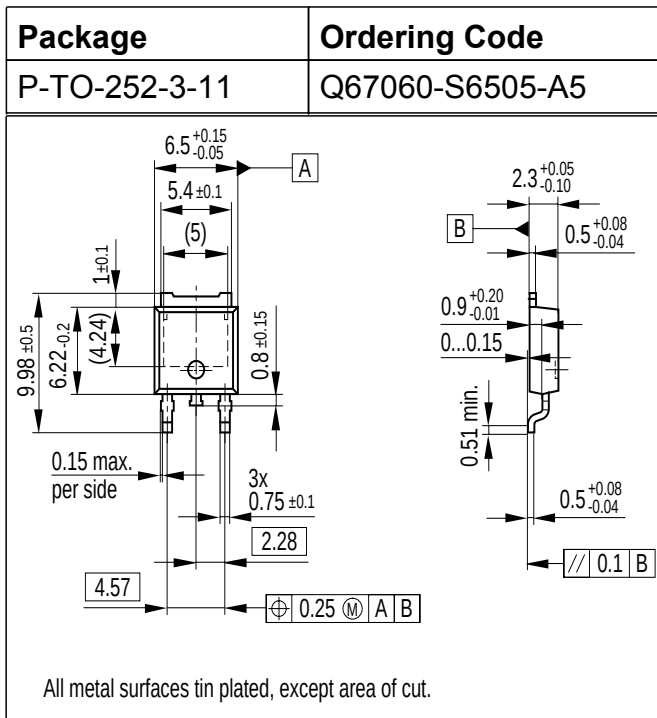


11 Determination of $I_{D(lim)}$

$I_{D(lim)} = f(t)$; $t_m = 200\mu\text{s}$

Parameter: T_{jstart}





Revision History : 2004-03-05
Previous version : 2003-04-22

Page	Subjects (major changes since last revision)
2, 4	Footnote 2 extended to $V_{in} < 0V$, E_{tot} and ΔT_{JT}
2, 3	Footnote 5 implemented to P_{tot} , $I_{D(nom)}$ and $I_{D(ISO)}$
2	ESD test condition changed from MIL STD 883D, methode 3015.7 and EOS/ESD assn. standard S5.1-1993 to Jedec Norm EIA/JESD22-A114-B, Section 4
2	Humidity category classification changed from DIN 40040 value E to J-STD-20-B value MSL1
2	climatic category changed from DIN IEC 68-1 to DIN EN 60068-1
3	$V_{IN(th)}$ test conditions from $I_D = 0.3mA$ to $I_D = 0.6mA$

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at <http://www.infineon.com>

HITFET[®], SIPMOS[®] are registered trademarks of Infineon Technologies AG.

Edition 2004-02-02

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany**

**© Infineon Technologies AG 2001
All Rights Reserved.**

Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.